RTL8169S-32/RTL8169S-64

INTEGRATED GIGABIT ETHERNET CONTROLLER (NIC)

DATASHEET

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This document is intended for use by the software engineer when programming for Realtek RTL8169S-32 & RTL8169S-64 controller chips. Information pertaining to the hardware design of products using these chips is contained in a separate document.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2003/03/20	First release.
1.1	2003/04/12	Revised pin name and pin assignments.
1.2	2003/06/24	Minor 233-pin TFBGA pin number corrections. IEEE 802.3z changed to IEEE 802.3ab in General Description.
1.3	2003/09/23	Add the voltage variation to DC characteristics.
1.4	2003/09/24	Remove "JTAG support" from the Features section. The RTL8169S does not support JTAG.

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1. General Description

The Realtek RTL8169S-32 and RTL8169S-64 combine a triple-speed IEEE 802.3 compliant media access controller (MAC) with a triple-speed Ethernet transceiver, 32(64*)-bit PCI bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, they offer high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The devices support the PCI v2.2 bus interface for host communications with power management and are compliant with the IEEE 802.3 specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. They support an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

They also support the Advanced Configuration and Power Interface (ACPI)--power management for modern operating systems that are capable of Operating System directed Power Management (OSPM)--to achieve the most efficient power management possible.

In addition to the ACPI feature, the RTL8169S-32 and RTL8169S-64 support remote wake-up (including AMD Magic Packet, Re-LinkOk, and Microsoft® Wake-up frame) in both ACPI and APM (Advanced Power Management) environments. Also, the LWAKE pin provides four different output signals including active high, active low, positive pulse, and negative pulse. The versatility of the LWAKE pin provides motherboards with Wake-On-LAN (WOL) functionality. To support WOL from a deep power down state (e.g. D3cold, i.e. main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8169S-32 and RTL8169S-64.

The RTL8169S is fully compliant with Microsoft® NDIS5 (IP, TCP, UDP) Checksum and Segmentation Task-offload features, and supports IEEE 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation as a server network card. The devices also boost their PCI performance by supporting PCI Memory Read Line & Memory Read Multiple when transmitting, and Memory Write and Invalidate when receiving. To better qualify as a server card, the RTL8169S-32 and RTL8169S-64 support the PCI Dual Address Cycle (DAC) command when the assigned buffers reside at a physical memory address higher than 4 Gigabytes.

** 233-PIN TFBGA package only.*

2. Features

- Integrated 10/100/1000 transceiver
- Auto-Negotiation with Next page capability
- Supports PCI 2.2, 32-bit/64-bit (RTL8169S-64 only), 33/66MHz
- Supports pair swap/polarity/skew correction
- Crossover Detection & Auto-Correction
- Wake-on-LAN and remote wake-up support
- Microsoft® NDIS5 Checksum Offload (IP, TCP, UDP) and largesend offload support
- Supports Full Duplex flow control (IEEE 802.3x)
- Fully compliant with IEEE 802.3, IEEE 802.3u, IEEE 802.3ab
- Supports IEEE 802.1Q VLAN tagging
- Serial EEPROM and/or Flash support
- 3.3V signaling, 5V PCI I/O tolerant
- Transmit/Receive FIFO (8K/64K) support
- Supports power down/link down power saving
- 128-pin QFP/233-pin TFBGA package

3. System Applications

- Gigabit Ethernet Network Interface Cards/Workstation Cards

4. Pin Assignments

4.1. 128-Pin QFP Pin Assignments

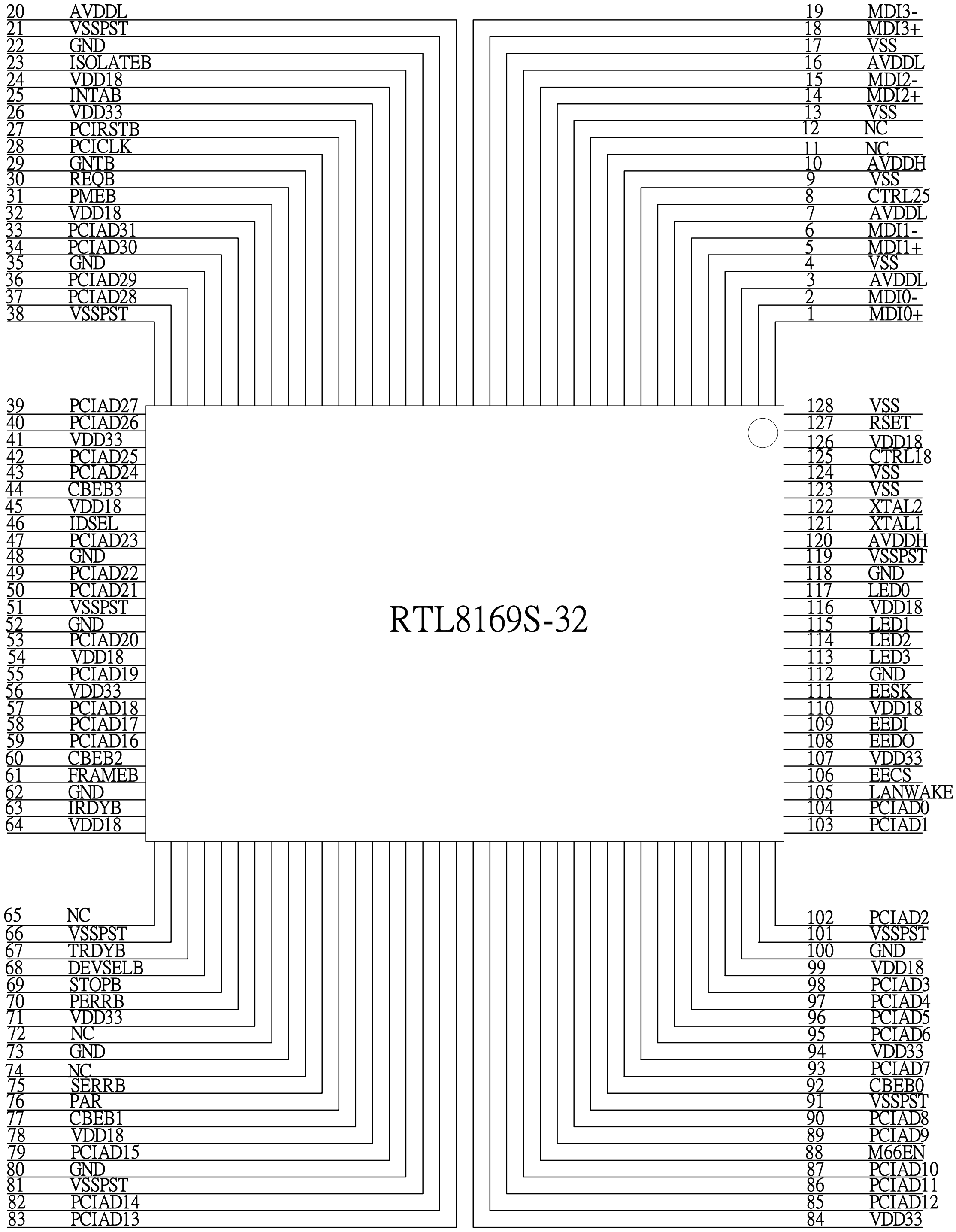


Figure 1. 128-Pin QFP Pin Assignments

4.2. 233-Pin TFBGA Pin Assignments

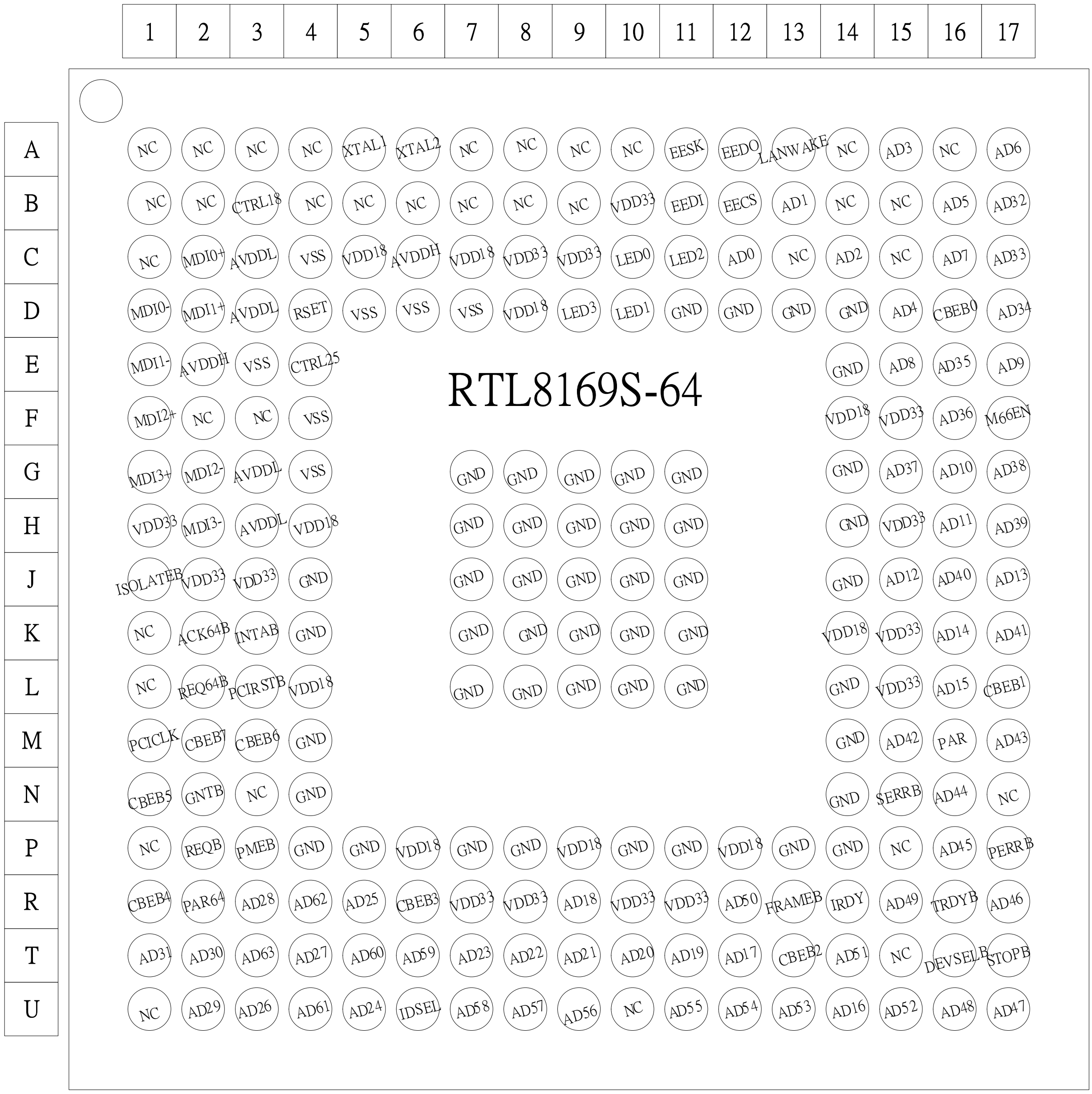


Figure 2. 233-Pin TFBGA Pin Assignments

5. Pin Descriptions

The following signal type codes are used in the tables:
I: Input.
O: Output
T/S: Tri-State bi-directional input/output pin.
S/T/S: Sustained Tri-State.
O/D: Open Drain.

5.1. *Power Management/Isolation*

Table 1. Power Management/Isolation

<table>
<tr><th>Symbol</th><th>Type</th><th>Pin No (128QFP)</th><th>Pin No (233BGA)</th><th>Description</th></tr>
<tr><td>PMEB
(PME#)</td><td>O/D</td><td>31</td><td>P3</td><td>Power Management Event: Open drain, active low.
Used to request a change in the current power management state and/or to indicate that a power management event has occurred.</td></tr>
<tr><td>ISOLATEB
(ISOLATE#)</td><td>I</td><td>23</td><td>J1</td><td>Isolate Pin: Active low.
Used to isolate the RTL8169S from the PCI bus. The RTL8169S will not drive its PCI outputs (excluding PME#) and will not sample its PCI input (including PCIRSTB and PCICLK) as long as the Isolate pin is asserted.</td></tr>
<tr><td>LANWAKE</td><td>O</td><td>105</td><td>A13</td><td>LAN WAKE-UP Signal (When CardB_En=0, bit2 Config3):
This signal is used to inform the motherboard to execute the wake-up process. The motherboard must support Wake-On-LAN (WOL). There are 4 choices of output that may be asserted from the LANWAKE pin (active high, active low, positive pulse, and negative pulse). We can configure the LANWAKE output via two CONFIG bits: LWACT(Config1.4) and LWPTN(Config4.2).
<table>
<tr><td colspan="2" rowspan="2">LWAKE Output</td><td colspan="2">LWACT</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td rowspan="2">LWPTN</td><td>0</td><td>Active high</td><td>Active low</td></tr>
<tr><td>1</td><td>Positive pulse</td><td>Negative pulse</td></tr>
</table>
The default output is an active high signal. Once a PME event is received, the LANWAKE and PMEB assert at the same time when the LWPME (bit4, CONFIG4) is set to 0. If the LWPME is set to 1, the LANWAKE asserts only when the PMEB asserts and ISOLATEB is low.</td></tr>
</table>

5.2. PCI Interface

Table 2. PCI Interface

Symbol	Type	Pin No. (128QFP)	Pin No. (233BGA)	Description
PCIADPIN63-32	T/S		T3, R4, U4, T5, T6, U7, U8, U9, U11, U12, U13, U15, T14, R12, R15, U16, U17, R17, P16, N16, M17, M15, K17, J16, H17, G17, G15, F16, E16, D17, C17, B17	**AD63-32: High 32-bit PCI address and data multiplexed pins.** Address and Data are multiplexed on the same pins and provide 32 additional bits. During an address phase (when using the DAC command and when REQ64B is asserted), the upper 32-bits of a 64-bit address are transferred; otherwise, these bits are reserved but are stable and undetermined. During a data phase, an additional 32-bits of data are transferred when a 64-bit transaction has been negotiated by the assertion of REQ64B and ACK64B.
PCIADPIN31-0	T/S	33, 34, 36, 37, 39, 40, 42, 43, 47, 49, 50, 53, 55, 57, 58, 59, 79, 82, 83, 85, 86, 87, 89, 90, 93, 95, 96, 97, 98, 102, 103, 104	T1, T2, U2, R3, T4, U3, R5, U5, T7, T8, T9, T10, T11, R9, T12, U14, L16, K16, J17, J15, H16, G16, E17, E15, C16, A17, B16, D15, A15, C14, B13, C12	**AD31-0: Low 32-bit PCI address and data multiplexed pins.** The address phase is the first clock cycle in which FRAMEB is asserted. During the address phase, AD31-0 contains a physical address (32 bits). For I/O, this is a byte address, and for configuration and memory, it is a double-word address. The RTL8169S supports both big-endian and little-endian byte ordering. Write data is stable and valid when IRDYB is asserted. Read data is stable and valid when TRDYB is asserted. Data I is transferred during those clocks where both IRDYB and TRDYB are asserted. **AD16-0:** Boot PROM Address Bus. These pins are used to access up to a 128k-byte flash memory or EPROM. **AD31-24:** Boot PROM data bus during Boot PROM mode.
CBEBPIN7-4	T/S		M2, M3, N1, R1	**PCI bus command and byte enables multiplexed pins.** During the address phase of a transaction, CBEBPIN7-4 define the bus command. During the data phase, CBEBPIN7-4 are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. CBEBPIN4 applies to byte 4, and CBEBPIN7 applies to byte 7.
CBEBPIN3-0	T/S	44, 60, 77, 92	R6, T13, L17, D16	**PCI bus command and byte enables multiplexed pins.** During the address phase of a transaction, CBEBPIN3-0 define the bus command. During the data phase, CBEBPIN3-0 are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. CBEBPIN0 applies to byte 0, and CBEBPIN3 applies to byte 3.

Symbol	Type	Pin No. (128QFP)	Pin No. (233BGA)	Description
PCICLK	I	28	M1	**PCI clock:** This clock input provides timing for all PCI transactions and is input for the PCI device. Supports up to a 66MHz PCI clock.
DEVSELB	S/T/S	68	T16	**Device Select:** As a bus master, the RTL8169S samples this signal to insure that a PCI target recognizes the destination address for the data transfer. As a target, the RTL8169S asserts this signal low when it recognizes its target address after FRAMEB is asserted.
FRAMEB	S/T/S	61	R13	**Cycle Frame:** As a bus master, this pin indicates the beginning and duration of an access. FRAMEB is asserted low to indicate the start of a bus transaction. While FRAMEB is asserted, data transfer continues. When FRAMEB is de-asserted, the transaction is in the final data phase. As a target, the device monitors this signal before decoding the address to check if the current transaction is addressed to it.
GNTB	I	29	N2	**Grant:** This signal is asserted low to indicate to the RTL8169S that the central arbiter has granted the ownership of the bus to the RTL8169S. This input is used when the device is acting as a bus master.
REQB	T/S	30	P2	**Request:** The RTL8169S will assert this signal low to request the ownership of the bus from the central arbiter.
IDSEL	I	46	U6	**Initialization Device Select**: This pin allows the device to identify when configuration read/write transactions are intended for it.
INTAB	O/D	25	K3	**Interrupt A:** Used to request an interrupt. It is asserted low when an interrupt condition occurs, as defined by the Interrupt Status, Interrupt Mask.
IRDYB	S/T/S	63	R14	**Initiator Ready**: This indicates the initiating agent's ability to complete the current data phase of the transaction. As a bus master, this signal will be asserted low when the device is ready to complete the current data phase transaction. This signal is used in conjunction with the TRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low. As a target, this signal indicates that the master has put data on the bus.
TRDYB	S/T/S	67	R16	**Target Ready:** This indicates the target agent's ability to complete the current phase of the transaction. As a bus master, this signal indicates that the target is ready for the data during write operations and with the data during read operations. As a target, this signal will be asserted low when the (slave) device is ready to complete the current data phase transaction. This signal is used in conjunction with the IRDYB signal. Data transaction takes place at the rising edge of CLK when both IRDYB and TRDYB are asserted low.

Symbol	Type	Pin No. (128QFP)	Pin No. (233BGA)	Description
PAR	T/S	76	M16	**Parity:** This signal indicates even parity across PCIADPIN31-0 and CBEB3-0 including the PAR pin. PAR is stable and valid one clock after each address phase. For data phase, PAR is stable and valid one clock after either IRDYB is asserted on a write transaction or TRDYB is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. As a bus master, PAR is asserted during address and write data phases. As a target, PAR is asserted during read data phases.
M66EN	I	88	F17	**66MHZ_ENABLE:** This pin indicates to the device whether the bus segment is operating at 66 or 33MHz. When this pin (active high) is asserted, the current PCI bus segment that the device resides on operates in 66-MHz mode. If this pin is de-asserted, the current PCI bus segment operates in 33-MHz mode.
PERRB	S/T/S	70	P17	**Parity Error:** This pin is used to report data parity errors during all PCI transactions except a Special Cycle. PERRB is driven active (low) two clocks after a data parity error is detected by the device receiving data, and the minimum duration of PERRB is one clock for each data phase with parity error detected.
SERRB	O/D	75	N15	**System Error:** If an address parity error is detected and Configuration Space Status register bit 15 (detected parity error) is enabled, the device asserts the SERRB pin low and bit 14 of the Status register in Configuration Space.
STOPB	S/T/S	69	T17	**Stop:** Indicates that the current target is requesting the master to stop the current transaction.
PCIRSTB	I	27	L3	**Reset:** When PCIRSTB is asserted low, the device performs an internal system hardware reset. PCIRSTB must be held for a minimum period of 120 ns.
ACK64B	S/T/S		K2	**Acknowledge 64-bit Transfer:** When actively driven by a device that has positively decoded its address as the target of the current access, indicates the target is willing to transfer data using 64 bits. ACK64B has the same timing as DEVSELB.
REQ64B	S/T/S		L2	**Request 64-bit Transfer:** When asserted by the current bus master, indicates it desires to transfer data using 64 bits. REQ64B also has the same timing as FRAMEB.
PAR64	T/S		R2	**Parity Upper DWORD** is an even parity bit that protects AD[64:32] and C/BE[7:4]. PAR64 must be valid one clock after each address phase on any transaction in which REQ64B is asserted.

5.3. EEPROM

Table 3. EEPROM

Symbol	Type	Pin No (128QFP)	Pin No (233BGA)	Description
EESK	O	111	A11	Serial data clock
EEDI/AUX	I	109	B11	**EEDI:** Serial data input **AUX:** Input pin to detect if Aux. Power exists or not on initial power-on. This pin should be connected to Boot PROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to aux. power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8169S assumes that no Aux. Power exists.
EEDO	O	108	A12	Serial data output
EECS/BROMCSB	O	106	B12	**EECS:** EEPROM chip select **BROMCSB:** This is the chip select signal of the Boot PROM.

5.4. Transceiver Interface

Table 4. Transceiver Interface

Symbol	Type	Pin No (128QFP)	Pin No (233BGA)	Description
MDI[0]+	I/O	1	C2	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDI[0]–	I/O	2	D1	
MDI[1]+	I/O	5	D2	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDI[1]–	I/O	6	E1	
MDI[2]+	I/O	14	F1	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDI[2]–	I/O	15	G2	
MDI[3]+	I/O	18	G1	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
MDI[3]–	I/O	19	H2	

5.5. Clock

Table 5. Clock

Symbol	Type	Pin No (128QFP)	Pin No (233BGA)	Description
Xtal1	I	121	A5	Input of 25MHz clock reference.
Xtal2	O	122	A6	output of 25MHz clock reference.

5.6. Regulator & Reference

Table 6. Regulator & Reference

Symbol	Type	Pin No (128QFP)	Pin No (233BGA)	Description
CTRL25	O	8	E4	Regulator Control. Voltage control to external 2.5V regulator.
CTRL18	O	125	B3	Regulator Control. Voltage control to external 1.8V regulator.
RSET	I	127	D4	Reference. External Resistor Reference.

5.7. LEDs

Table 7. LEDs

<table>
<tr><th>Symbol</th><th>Type</th><th>Pin No (128QFP)</th><th>Pin No (233BGA)</th><th>Description</th></tr>
<tr><td>LED0/ BROMOEB</td><td>O</td><td>117</td><td>C10</td><td rowspan="4">
<table>
<tr><th>LEDS1-0</th><th>00</th><th>01</th><th>10</th><th>11</th></tr>
<tr><td>LED0</td><td>Tx/Rx</td><td>ACT(Tx/Rx)</td><td>Tx</td><td>LINK10/ ACT</td></tr>
<tr><td>LED1</td><td>LINK 100</td><td>LINK10/100 /1000</td><td>LINK10/100 /1000</td><td>LINK100/ ACT</td></tr>
<tr><td>LED2</td><td>LINK 10</td><td>FULL</td><td>Rx</td><td>FULL</td></tr>
<tr><td>LED3</td><td>LINK 1000</td><td>-</td><td>FULL</td><td>LINK1000/ ACT</td></tr>
</table>
BROMOEB: This enables the output buffer of the Boot PROM or Flash memory during a read operation.
</td></tr>
<tr><td>LED1</td><td>O</td><td>115</td><td>D10</td></tr>
<tr><td>LED2</td><td>O</td><td>114</td><td>C11</td></tr>
<tr><td>LED3</td><td>O</td><td>113</td><td>D9</td></tr>
</table>

Note 1: During power down mode, the LED signals are logic high.

Note 2: LEDS1-0's initial value comes from 93C46/93C56.

5.8. Power & Ground

Table 8. Power & Ground

Symbol	Type	Pin No (128QFP)	Pin No (233BGA)	Description
VDD18	Power	24, 32, 45, 54, 64, 78, 99, 110, 116,126	C5, C7, D8, F14, H4, K14, L4, P6, P9, P12	Digital 1.8V power supply.
VDD33	Power	26, 41, 56, 71, 84, 94, 107	B10, C8, C9, F15, H1, H15, J2, J3, K15, L15, R7, R8, R10, R11	Digital 3.3V power supply.
GND/VSSPST	Power	21, 22, 35, 38, 48, 51, 52, 62, 66, 73, 80, 81, 91, 100, 101, 112, 118, 119	D11, D12, D13, D14, E14, G7, G8, G9, G10, G11, G14, H7, H8, H9, H10, H11, H14, J4, J7, J8, J9, J10, J11, J14, K4, K7, K8, K9, K10, K11, L7, L8, L9, L10, L11, L14, M4, M14, N4, N14, P4, P5, P7, P8, P10, P11, P13, P14	Digital Ground
AVDDL	Power	3, 7, 16, 20	C3, D3, G3, H3	Analog 2.5V power supply.
AVDDH	Power	10, 120	E2, C6	Analog 3.3V power supply.
VSS	Power	4, 9, 13, 17, 123, 124, 128	F4, G4, C4, D5, D6, D7, E3	Analog Ground

5.9. NC (Not Connected)

Table 9. NC (Not Connected)

Symbol	Type	Pin No (128QFP)	Pin No (233BGA)	Description
NC		11, 12, 65, 72, 74	A1, A2, A3, A4, A7, A8, A9, A10, A14, A16, B1, B2, B4, B5, B6, B7, B8, B9, B14, B15, C1, C13, C15, F2, F3, K1, L1, N3, N17, P1, P15, T15, U1, U10	Not Connected.

6. Functional Description

6.1. Transceiver

6.1.1. Transmitter

In 10M mode, the Tx MAC retrieves packet data from the Tx Buffer Manager and sends it out through the transmitting physical layer interface. The transmit 4-bit nibbles (TXD[3:0]) clocked at 2.5Mhz (TXC), are serialized into 10Mbps serial data. Then, the 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the DAC converter.

In 100M mode, the transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25Mhz (TXC), are converted into 5B symbol code via 4B/5B coding technology, scrambling, and serializing before being converted to 125Mhz NRZ and NRZI signals. After that, the NRZI signal is passed to the MLT3 encoder, then to the DAC converter for transmission onto the media.

In 1000M mode, the RTL8169S's PCS layer receives data bytes from the MAC through the GMII interface and performs the generation of continuous code-groups through 4D-PAM5 coding technology. Then, those code groups are passed through waveform shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT5 cable at 125MBaud/s through DAC converter.

6.1.2. Receiver

In MII (10Mbps) mode, the received differential signal is converted into a Manchester-encoded data stream. The stream is processed with a Manchester decoder, and is de-serialized into 4-bit wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz. In 100Mbps mode, the MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and then is presented to the MII interface in 4-bit wide nibbles at a clock speed of 25MHz.

In GMII mode, the input signal from the media first passes through the on-chip sophisticated hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. Afterwards, the received signal is processed with adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. Then, the 8-bit wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the receive MII/GMII interface and sends it to the Rx Buffer Manager.

6.2. MAC

The RTL8169S supports new descriptor-based buffer management that significantly reduces host CPU utilization and is particularly effective in server applications. The new buffer management algorithm provides Microsoft Large-Send offload, IP checksum offload, TCP checksum offload, UDP checksum offload, and IEEE 802.1P, 802.1Q VLAN tagging capabilities. The device supports up to 1024 consecutive descriptors in memory for transmit and receive separately, which means there might be 3 descriptor rings, one a high priority transmit descriptor ring, another a normal priority transmit descriptor ring, and the other a receive descriptor ring. Each descriptor ring may consist of up to 1024 consecutive descriptors. Each descriptor consists of 4 consecutive double words. The start address of each descriptor ring should be 256-byte aligned. Software must pre-allocate enough buffers and configure all descriptor rings before transmitting and/or receiving packets. Descriptors can be chained to form a packet in both Tx and Rx. Refer to the Realtek RTL8169S Programming Guide for detailed information. Any Tx buffers pointed to by the Tx descriptors should be at least 4 bytes.

The RTL8169S will automatically pad any packets less than 64 bytes to 64-bytes long (including a 4-byte CRC) before transmitting that packet onto the network medium. If a packet consists of two or more descriptors, then the descriptors in command mode should have the same configuration, except EOR, FS, LS bits.

6.3. Next Page

If 1000Base-T mode is advertised, three additional Next Pages are automatically exchanged between the two link partners. Users can set Reg4.15 to 1 to exchange extra Next Pages via Reg7 and Reg8 as defined in IEEE 802.3ab.

6.4. MII/GMII Interface

6.4.1. MII

The RTL8169S supports 10Mbps and 100Mbps link operation. During the operation, the PHY communicates with the MAC through the MII as defined in the IEEE 802.3 (clause 22) specifications. The MII consists of a transmit data interface (TxEN, TxER, TXD[3:0], and TxCLK), a receive data interface (RxDV, RxER, RXD[3:0], and RxCLK), two status signals (CRS and COL) and a management interface (MDC and MDIO). In this mode of operation, both Transmit and Receive clocks are supplied by the PHY.

6.4.2. GMII

In 1000Base-T mode, the GMII interface is selected, the 125MHz transmit clock is expected on GTXCLK, TXCLK sources 25MHz, 2.5MHz, or 0MHz clock depending on the operation mode, and RXCLK sources the 125MHz receive clock.

6.5. LEDs

The RTL8169S supports four LED signals in four different configurable operation modes. The modes are shown in Pin Descriptions, page 5.

6.5.1. Link Monitor

The Link Monitor senses a link, such as LINK10, LINK100, LINK1000, LINK10/100/1000. Whenever a link is established, the specific link LED pin is driven low. Once disconnected, the link LED pin is driven high indicating that no network connection exists.

6.5.2. RX LED

In 10/100/1000Mbps mode, blinking of the Rx LED indicates that receive activity is occurring.

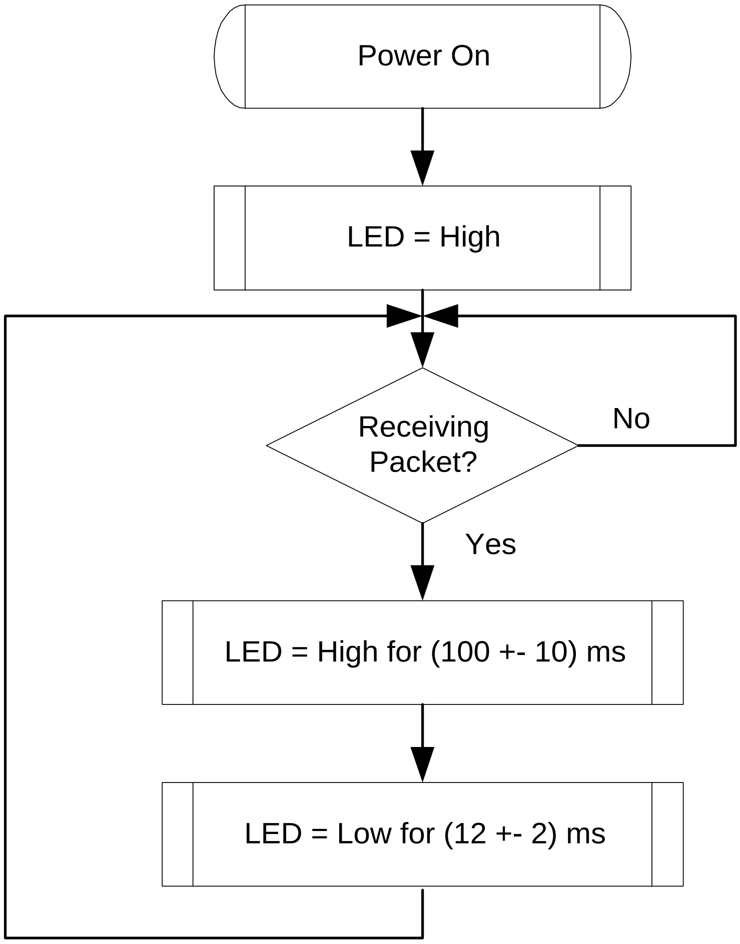


Figure 3. RX LED

6.5.3. TX LED

In 10/100/1000Mbps mode, blinking of the Tx LED indicates that transmit activity is occurring.

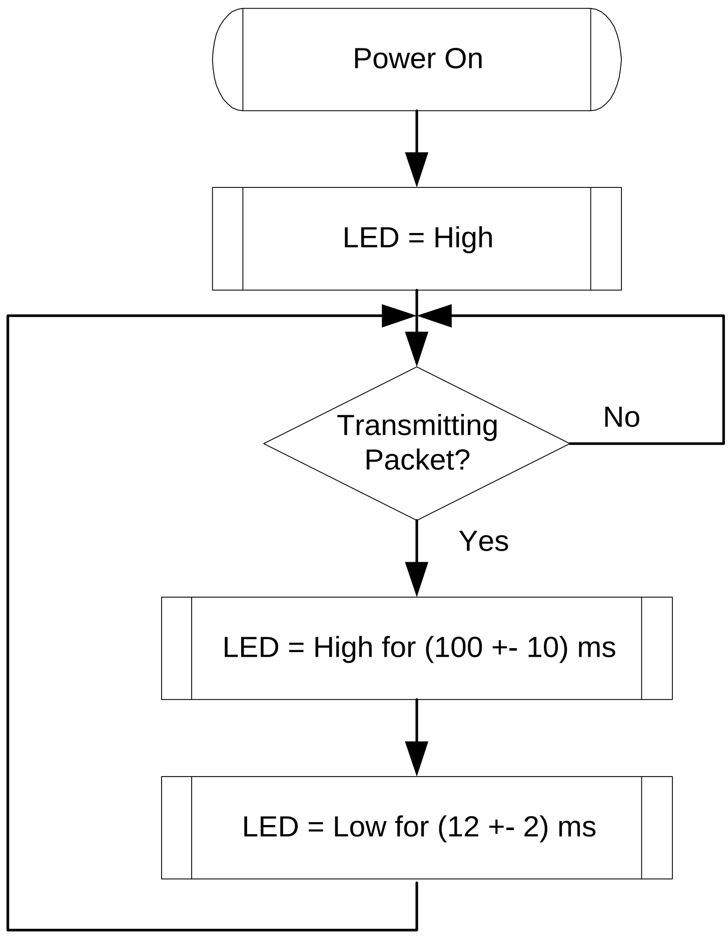


Figure 4. TX LED

6.5.4. TX/RX LED

In 10/100/1000Mbps mode, blinking of the Tx/Rx LED indicates that both transmit and receive activity is occurring.

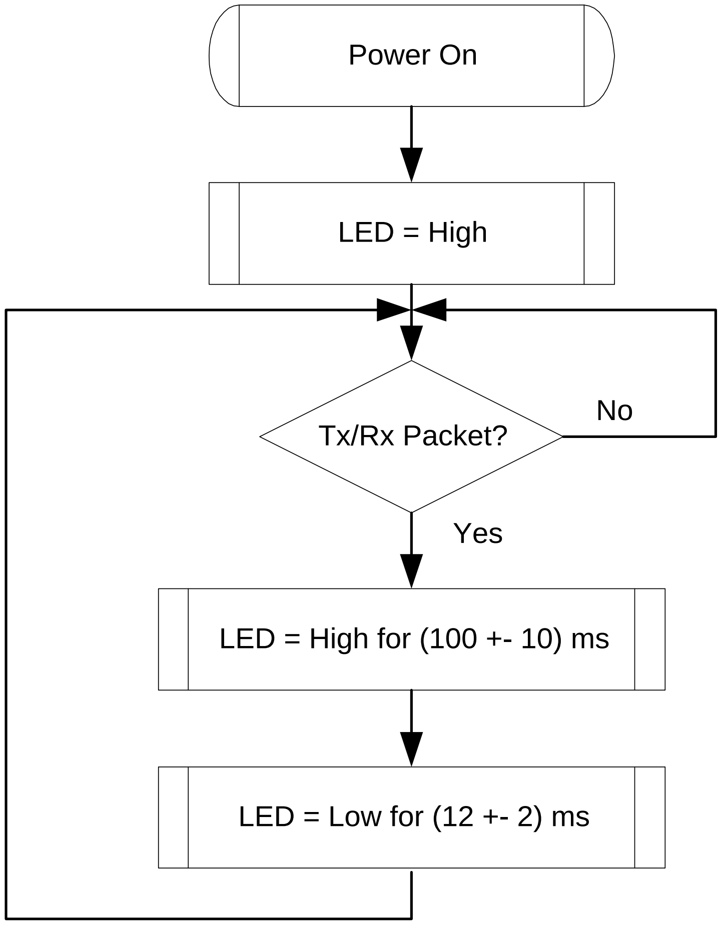


Figure 5. TX/RX LED

6.5.5. LINK/ACT LED

In 10/100/1000Mbps mode, blinking of the LINK/ACT LED indicates that the RTL8169S is linked and operating properly. When this LED is high for extended periods, it indicates that a link problem exists.

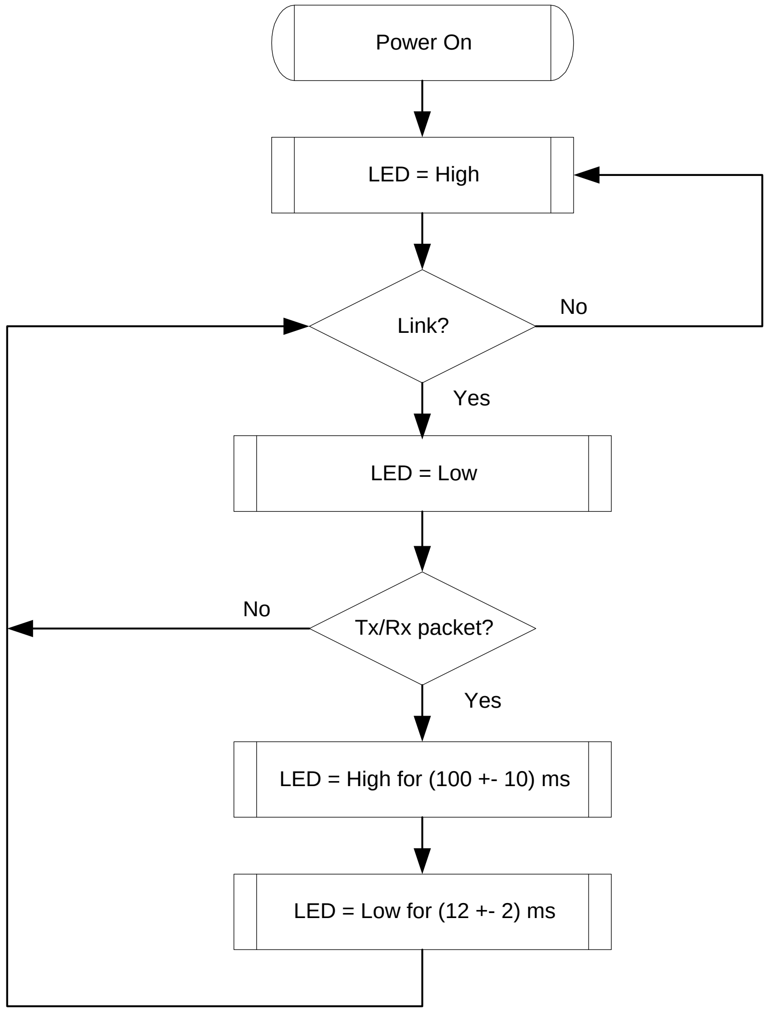


Figure 6. LINK/ACT LED

6.6. *Flash/EEPROM Interface*

The Flash interface consists of address bus MA(16:0) and data bus MD(7:0) which share the pin with PCI interface AD(16:0) and AD(32:24), respectively. It also consists of several control signals: WEB, OEB(LED0), CSB(EECS). The RTL8169S supports the attachment of an external EEPROM. The 93C46 is a 1K-bit EEPROM (the 93C56 is a 2K-bit EEPROM).

The EEPROM interface provides the ability for the RTL8169S to read from and write data to an external serial EEPROM device. Values in the external EEPROM allow default fields in PCI configuration space and I/O space to be overridden following a reboot or software EEPROM auto load command. The RTL8169S will auto load values from the EEPROM. If the EEPROM is not present, the RTL8169S initialization uses default values for the appropriate Configuration and Operational

Registers. Software can read and write to the EEPROM using “bit-bang” accesses via the 9346CR Register. The interface consists of EESK, EECS, EEDO, and EEDI.

Table 10. Flash/EEPROM Interface

Flash	Description
MA[16:0] (PCIAD16:0)	Boot PROM Address Bus. These pins are used to access up to a 128k-byte flash memory or EEPROM.
MD7-0(PCIAD31:24)	Boot PROM data bus when in Boot PROM mode.
CSB(EECS/BROMCSB)	The chip select signal of the Boot PROM.
OEB(LED0/BROMOEB)	Enables the output buffer of the Boot PROM or Flash memory during a read operation.
EEPROM	**Description**
EECS	93C46 (93C56) chip select
EESK	EEPROM serial data clock
EEDI/Aux	Input data bus/Input pin to detect if Aux. Power exists or not on initial power-on. This pin should be connected to Boot PROM. To support wakeup from ACPI D3cold or APM power-down, this pin must be pulled high to aux. power via a resistor. If this pin is not pulled high to Aux. Power, the RTL8169S assumes that no Aux. Power exists.
EEDO	Output data bus

6.7. Power Management

The RTL8169S is compliant with ACPI (Rev 1.0, 1.0b, 2.0), PCI Power Management (Rev 1.1), and Network Device Class Power Management Reference Specification (V1.0a), such as to support an OS-directed Power Management (OSPM) environment.

The RTL8169S can monitor the network for a Wakeup Frame, a Magic Packet, or a Re-LinkOk, and notify the system via PME# when such a packet or event occurs. Then, the whole system can be restored to a normal state to process incoming jobs.

When the RTL8169S is in power down mode (D1 ~ D3):

- The Rx state machine is stopped, and the RTL8169S monitors the network for wakeup events such as a Magic Packet, Wakeup Frame, and/or Re-LinkOk, in order to wake up the system. When in power down mode, the RTL8169S will not reflect the status of any incoming packets in the ISR register and will not receive any packets into the Rx FIFO buffer.
- The FIFO status and packets that have already been received into the Rx FIFO before entering power down mode are held by the RTL8169S.
- Transmission is stopped. PCI bus master mode is stopped. The Tx FIFO buffer is held.
- After restoration to a D0 state, the RTL8169S transfers data that was not moved into the Tx FIFO buffer during power down mode. Packets that were not transmitted completely last time are re-transmitted.

The D3cold_support_PME bit (bit15, PMC register) and the Aux_I_b2:0 bits (bit8:6, PMC register) in PCI configuration space depend on the existence of Aux power (bit15, PMC) = 1.
If EEPROM D3cold_support_PME bit (bit15, PMC) = 0, the above 4 bits are all 0's.
Example:

If EEPROM D3c_support_PME = 1:

- If Aux. power exists, then PMC in PCI config space is the same as EEPROM PMC
  (if EEPROM PMC = C2 F7, then PCI PMC = C2 F7)
- If Aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's
  (if EEPROM PMC = C2 F7, the PCI PMC = 02 76)

In the above case, if wakeup support is desired when main power is off, it is suggested that the EEPROM PMC be set to C2 F7 (Realtek EEPROM default value).

If EEPROM D3c_support_PME = 0:

- If Aux. power exists, then PMC in PCI config space is the same as EEPROM PMC
  (if EEPROM PMC = C2 77, then PCI PMC = C2 77)
- If Aux. power is absent, then PMC in PCI config space is the same as EEPROM PMC except the above 4 bits are all 0's.
  (if EEPROM PMC = C2 77, then PCI PMC = 02 76)

In the above case, if wakeup support is not desired when main power is off, it is suggested that the EEPROM PMC be set to 02 76.

Link Wakeup occurs only when the following conditions are met:

- The LinkUp bit (CONFIG3#4) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the PME# can be asserted in the current power state.
- The Link status is re-established.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8169S, e.g. a broadcast, multicast, or unicast packet addressed to the current RTL8169S adapter.
- The received Magic Packet does not contain a CRC error.
- The Magic bit (CONFIG3#5) is set to 1, the PMEn bit (CONFIG1#0) is set to 1, and the PME# can be asserted in the current power state.
- The Magic Packet pattern matches, i.e. 6 * FFh + MISC (can be none) + 16 * DID(Destination ID) in any part of a valid (Fast) Ethernet packet.

A Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8110S, e.g. a broadcast, multicast, or unicast address to the current RTL8110S adapter.
- The received Wakeup Frame does not contain a CRC error.
- The PMEn bit (CONFIG1#0) is set to 1.
- The 16-bit CRC* of the received Wakeup Frame matches with the 16-bit CRC* of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8169S is configured to allow direct packet wakeup, e.g. a broadcast, multicast, or unicast network packet.

*16-bit CRC: The RTL8169S supports two normal wakeup frames (covering 64 mask bytes from offset 0 to 63 of any incoming network packet) and three long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet).

The PME# signal is asserted only when the following conditions are met:

1. The PMEn bit (bit0, CONFIG1) is set to 1.
2. The PME_En bit (bit8, PMCSR) in PCI Configuration Space is set to 1.
3. The RTL8169S may assert PME# in the current power state or in isolation state, depending on the PME_Support (bit15-11) setting of the PMC register in PCI Configuration Space.
4. A Magic Packet, LinkUp, or Wakeup Frame been received.
5. Writing a 1 to the PME_Status (bit15) of the PMCSR register in the PCI Configuration Space clears this bit and causes the RTL8169S to stop asserting a PME# (if enabled).

When the device is in power down mode, e.g. D1-D3, the IO, MEM, and Boot ROM spaces are all disabled. After a RST# assertion, the device's power state is restored to D0 automatically if the original power state was $D3_{cold}$. There is no hardware delay at the device's power state transition. When in ACPI mode, the device does not support PME (Power Management Enable) from D0 (this is the Realtek default setting of the PMC register auto loaded from EEPROM). The setting may be changed from the EEPROM, if required). The RTL8169S also supports the legacy LAN WAKE-UP function. The LWAKE pin is used to notify legacy motherboards to execute the wake-up process whenever the device receives a wakeup event, such as Magic Packet.

The LWAKE signal is asserted according to the following settings:

1. LWPME bit (bit4, CONFIG4):

- LWAKE can only be asserted when the PMEB is asserted and the ISOLATEB is low.
- LWAKE is asserted whenever a wakeup event occurs.

2. Bit1 of DELAY byte (offset 1Fh, EEPROM):

- LWAKE signal is enabled.
- LWAKE signal is disabled.

7. Characteristics

7.1. *Absolute Maximum Ratings*

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 11. Absolute Maximum Ratings

Description/Symbol	Minimum	Maximum	Unit
Supply Voltage (VDD33, AVDDH)	-0.5	4	V
Supply Voltage (VDD25)	-0.5	3	V
Supply Voltage (VDD18)	-0.5	2	V
Input Voltage (DCinput)	-0.5	VDD33 + 0.5	V
Output Voltage (DCoutput)	-0.5	VDD33 + 0.5	V
Storage Temperature	-55	+125	°C

7.2. *Recommended Operating Conditions*

Table 12. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	VDD33, AVDDH	3.0	3.3	3.6	V
	VDD25	2.25	2.5	2.75	V
	VDD18	1.67	1.8	1.92	V
Ambient Temperature T_A		0		70	°C
Maximum Junction Temperature				125	°C

7.3. *Crystal Requirements*

Table 13. Crystal Requirements

Symbol	Description/Condition	Minimum	Typical	Maximum	Unit
F_{ref}	Parallel resonant crystal reference frequency, fundamental mode, AT-cut type.		25		MHz
F_{ref} Stability	Parallel resonant crystal frequency stability, fundamental mode, AT-cut type. T_a=25℃.	-50		+50	ppm
F_{ref} Tolerance	Parallel resonant crystal frequency tolerance, fundamental mode, AT-cut type. T_a=-20℃~+70℃.	-30		+30	ppm
F_{ref} Duty Cycle	Reference clock input duty cycle	40		60	%
C_L	Load Capacitance				pF
ESR	Equivalent Series Resistance				Ω
DL	Drive Level			0.5	mW

7.4. Thermal Characteristics

Table 14. Thermal Characteristics

Parameter	Minimum	Maximum	Units
Storage temperature	-55	+125	°C
Operating temperature	0	70	°C

7.5. DC Characteristics

Table 15. DC Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD33	3.3V Supply Voltage		3.0	3.3	3.6	V
VDD18	1.8V Supply Voltage		1.67	1.8	1.92	V
VDD25	2.5V Supply Voltage		2.25	2.5	2.75	V
V_{oh}	Minimum High Level Output Voltage	I_{oh} = -8mA	0.9 * Vcc		Vcc	V
V_{ol}	Maximum Low Level Output Voltage	I_{ol} = 8mA			0.1 * Vcc	V
V_{ih}	Minimum High Level Input Voltage		0.5 * Vcc		Vcc+0.5	V
V_{il}	Maximum Low Level Input Voltage		-0.5		0.3 * Vcc	V
I_{in}	Input Current	V_{in} = V_{cc} or GND	-1.0		1.0	uA
I_{oz}	Tri-State Output Leakage Current	V_{out} = V_{cc} or GND	-10		10	uA
Icc33	Average Operating Supply Current from 3.3V					mA
I_{cc18}	Average Operating Supply Current from 1.8V					mA

7.6. AC Characteristics

7.6.1. Serial EEPROM Interface Timing

93C46(64*16)/93C56(128*16)

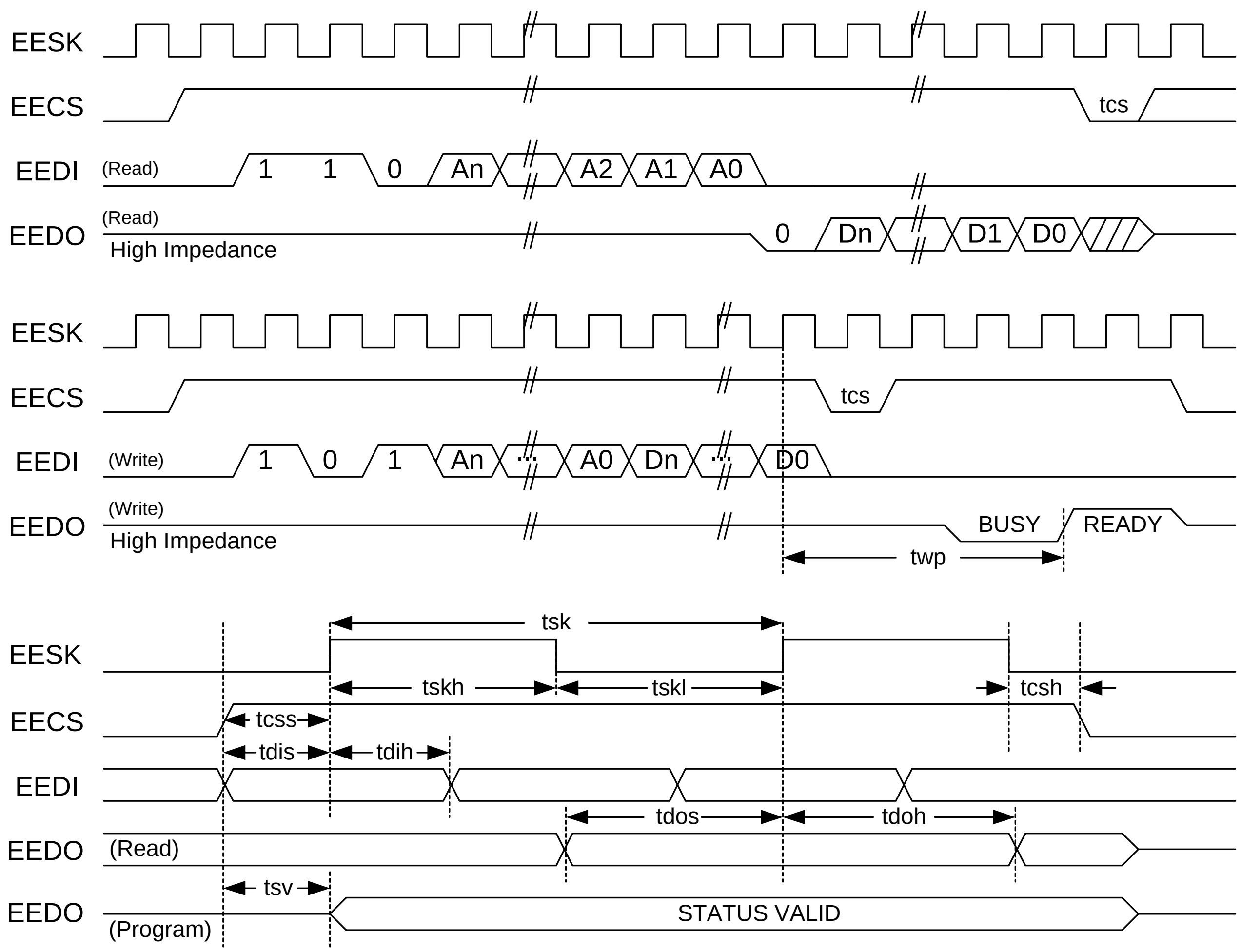


Figure 7. Serial EEPROM Interface Timing

Table 16. EEPROM Access Timing Parameters

Symbol	Parameter	EEPROM Type	Min.	Max.	Unit
tcs	Minimum CS Low Time	9346/9356	1000/250		ns
twp	Write Cycle Time	9346/9356		10/10	ms
tsk	SK Clock Cycle Time	9346/9356	4/1		us
tskh	SK High Time	9346/9356	1000/500		ns
tskl	SK Low Time	9346/9356	1000/250		ns
tcss	CS Setup Time	9346/9356	200/50		ns
tcsh	CS Hold Time	9346/9356	0/0		ns

Symbol	Parameter	EEPROM Type	Min.	Max.	Unit
tdis	DI Setup Time	9346/9356	400/50		ns
tdih	DI Hold Time	9346/9356	400/100		ns
tdos	DO Setup Time	9346/9356	2000/500		ns
tdoh	DO Hold Time	9346/9356		2000/500	ns
tsv	CS to Status Valid	9346/9356		1000/500	ns

7.7. PCI Bus Operation Timing

7.7.1. PCI Bus Timing Parameters

Table 17. PCI Bus Timing Parameters

		66MHz		33MHz		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Symbol**	**Parameter**
T val	CLK to Signal Valid Delay-bused signals	2	6	2	11	ns
T val (ptp)	CLK to Signal Valid Delay-point to point	2	6	2	12	ns
T on	Float to Active Delay	2		2		ns
T off	Active to Float Delay		14		28	ns
T su	Input Setup Time to CLK-bused signals	3		7		ns
T su (ptp)	Input Setup Time to CLK-point to point	5		10		ns
T h	Input Hold Time from CLK	0		0		ns
T rst	Reset active time after power stable	1		1		ms
T rst-clk	Reset active time after CLK STABLE	100		100		us
T rst-off	Reset Active to Output Float delay		40		40	ns
T rrsu	REQB to REQ64B Setup Time	10*Tcyc		10*Tcyc		ns
T rrh	RSTB to REQ64B Hold Time	0	50	0	50	ns
T rhfa	RSTB High to First configuration Access	2^25		2^25		clocks
T rhff	RSTB High to First FRAMEB assertion	5		5		clocks

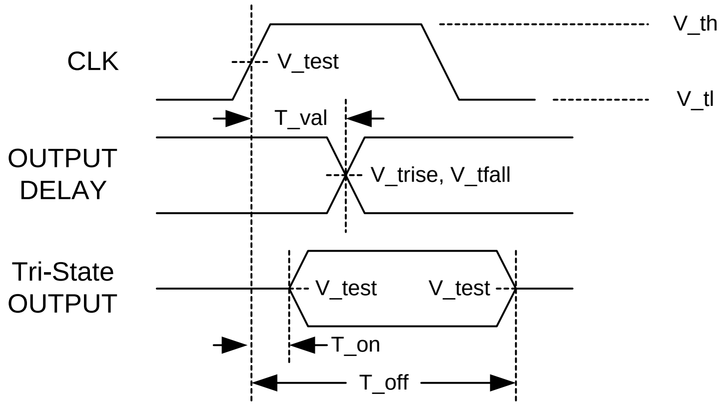


Figure 8. Output Timing Measurement Conditions

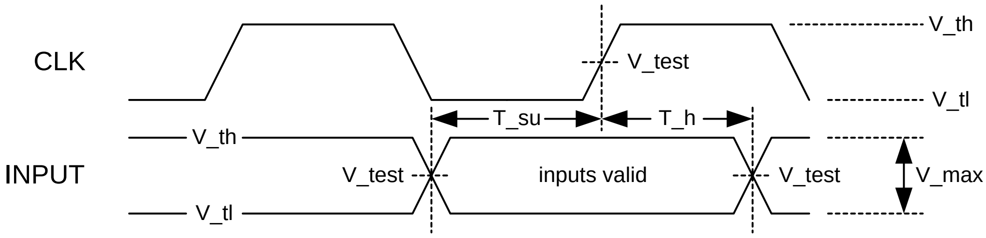


Figure 9. Input Timing Measurement Conditions

Table 18. Measurement Condition Parameters

Symbol	Level	Units
Vth	0.6Vcc	V
Vtf	0.2Vcc	V
Vtest	0.4Vcc	V
Vtrise	0.285Vcc	V
Vtfall	0.615Vcc	V
Vmax	0.4Vcc	V
Input Signal Edge Rate	1	V/ns

7.7.2. PCI Clock Specification

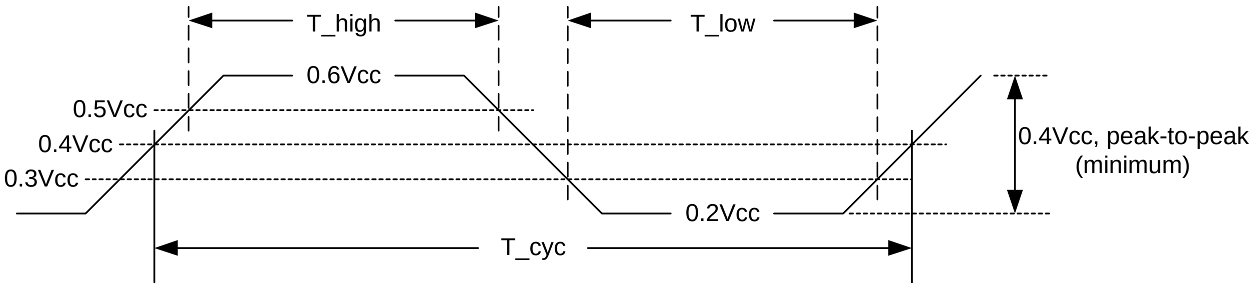


Figure 10. 3.3V Clock Waveform

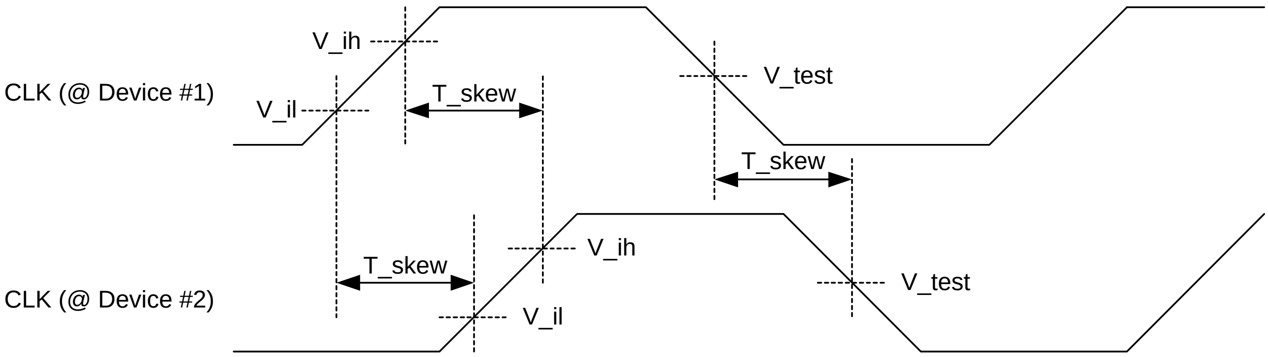


Figure 11. Clock Skew Diagram

Table 19. Clock and Reset Specifications

		66MHz		33MHz		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Symbol**	**Parameter**
Tcyc	CLK Cycle Time	15	30	30	∞	ns
Thigh	CLK High Time	6		11		ns
Tlow	CLK Low Time	6		11		ns
--	CLK Slew Rate	1.5	4	1	4	V/ns
--	RST# Slew Rate	50	-	50	-	mV/ns
Tskew	CLK Skew		1		2	ns

7.7.3. PCI Transactions

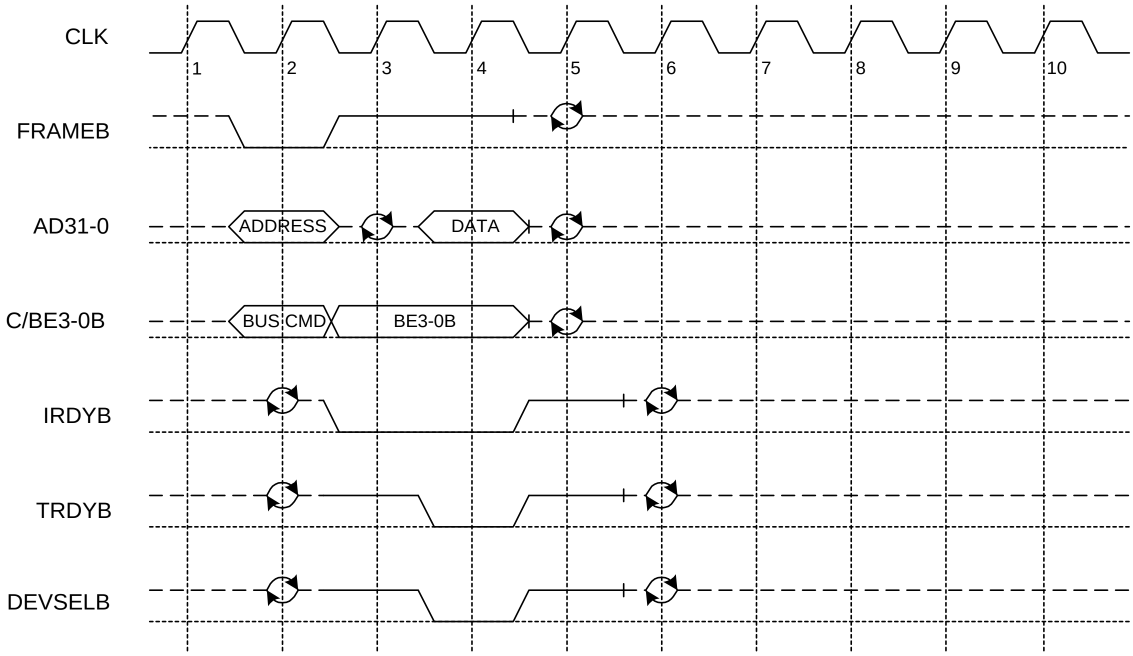


Figure 12. I/O Read

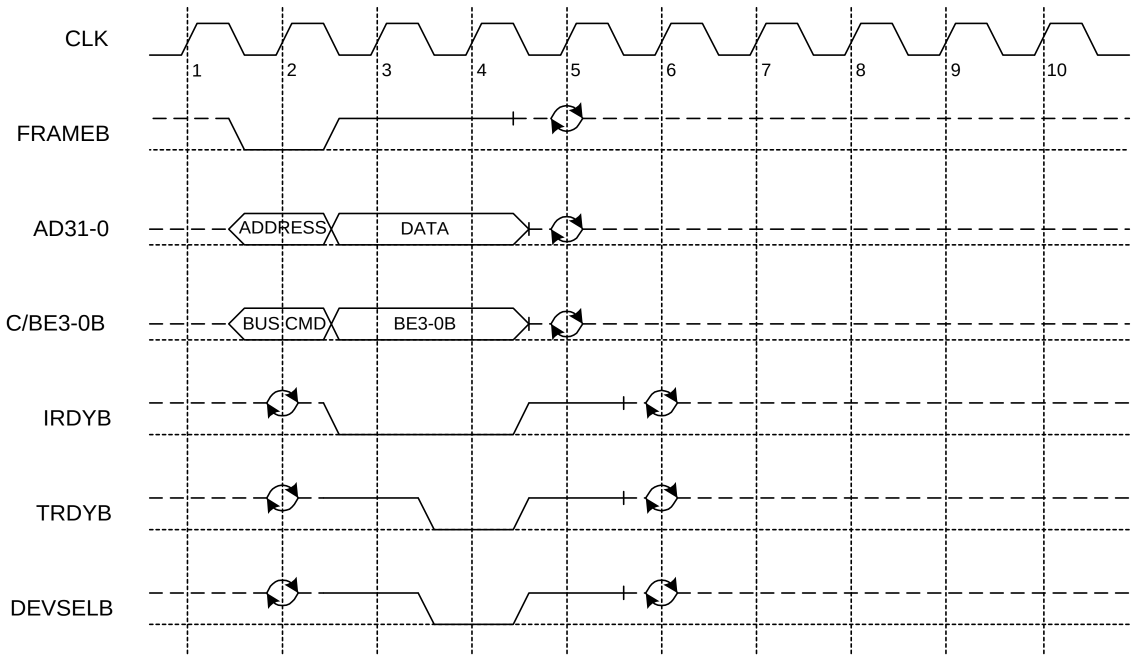


Figure 13. I/O Write

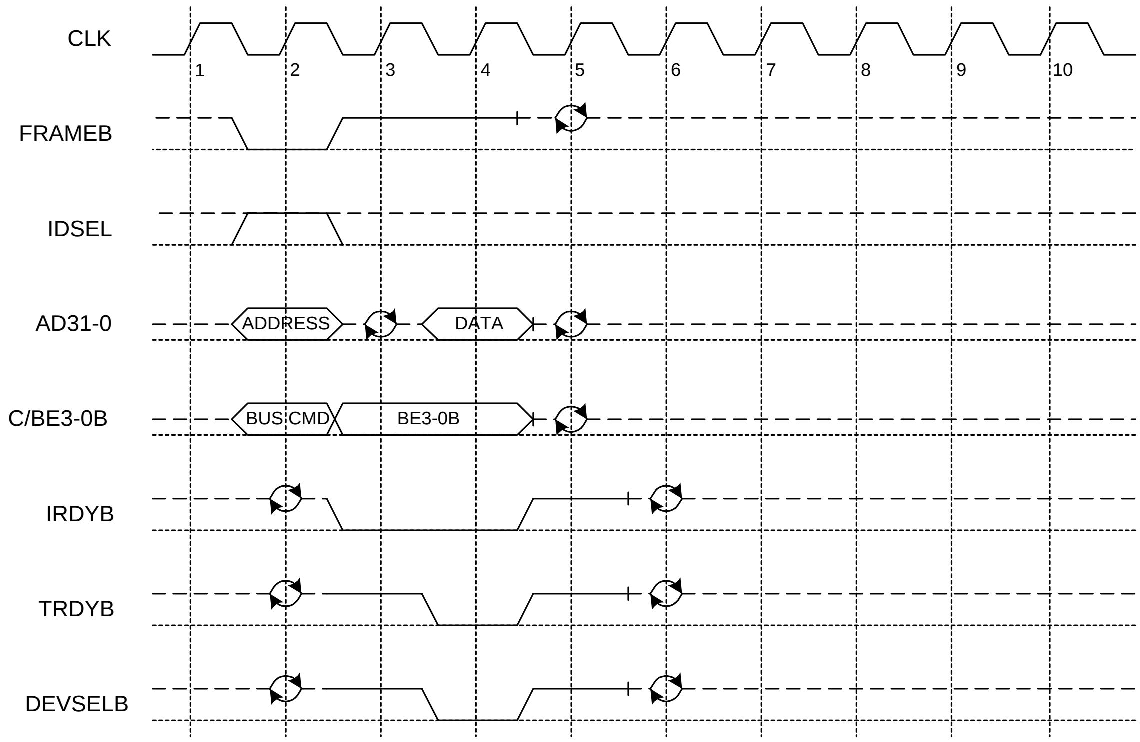


Figure 14. Configuration Read

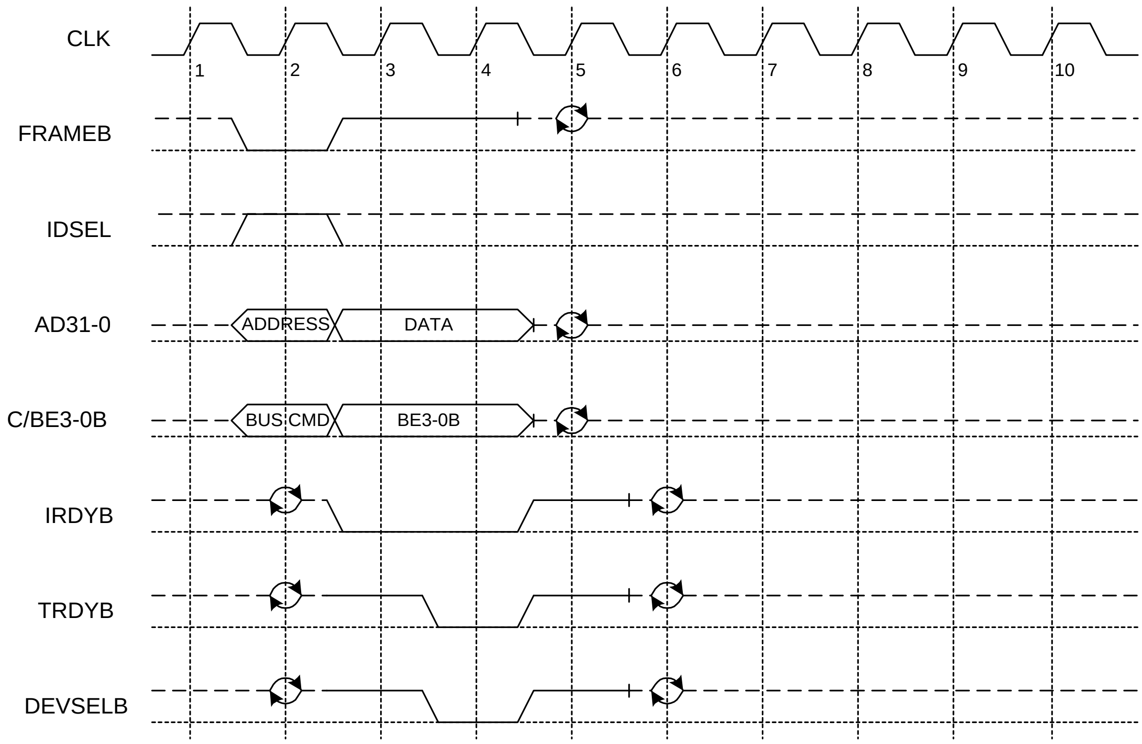


Figure 15. Configuration Write

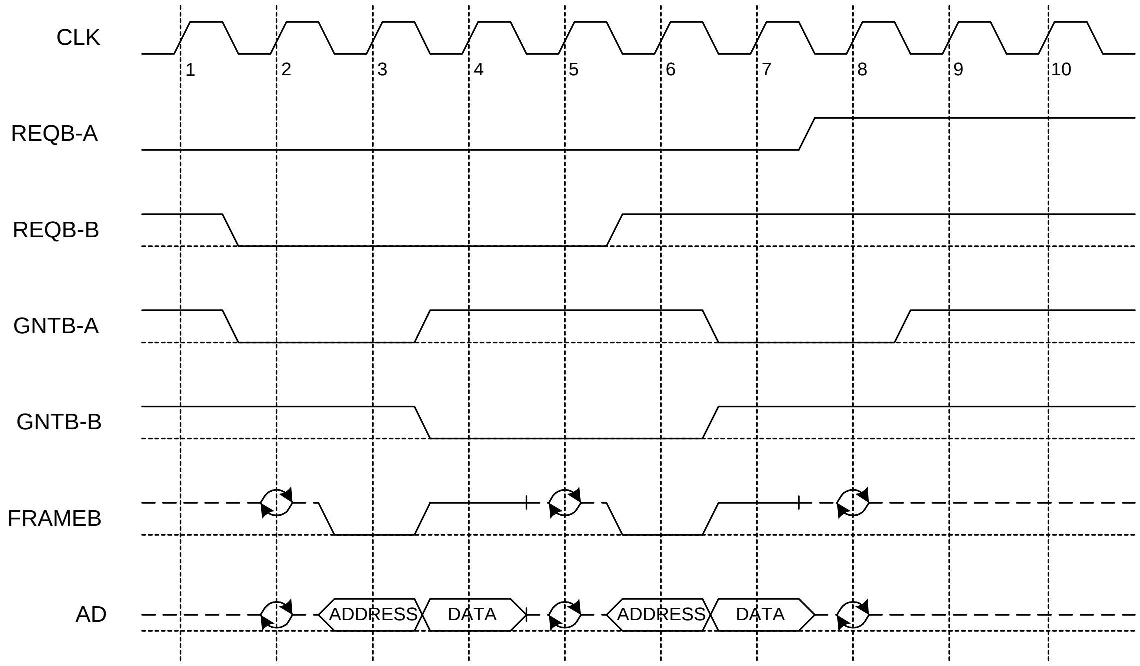


Figure 16. Bus Arbitration

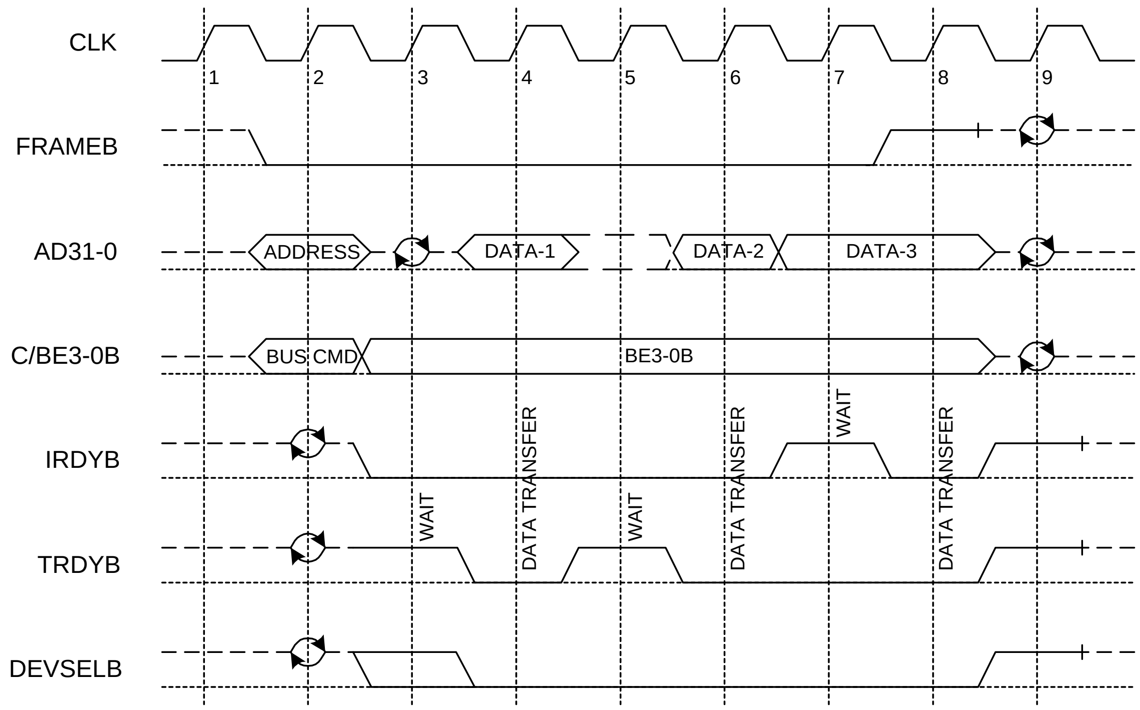


Figure 17. Memory Read below 4GB (32-bit address, 32-bit data; 32-bit slot)

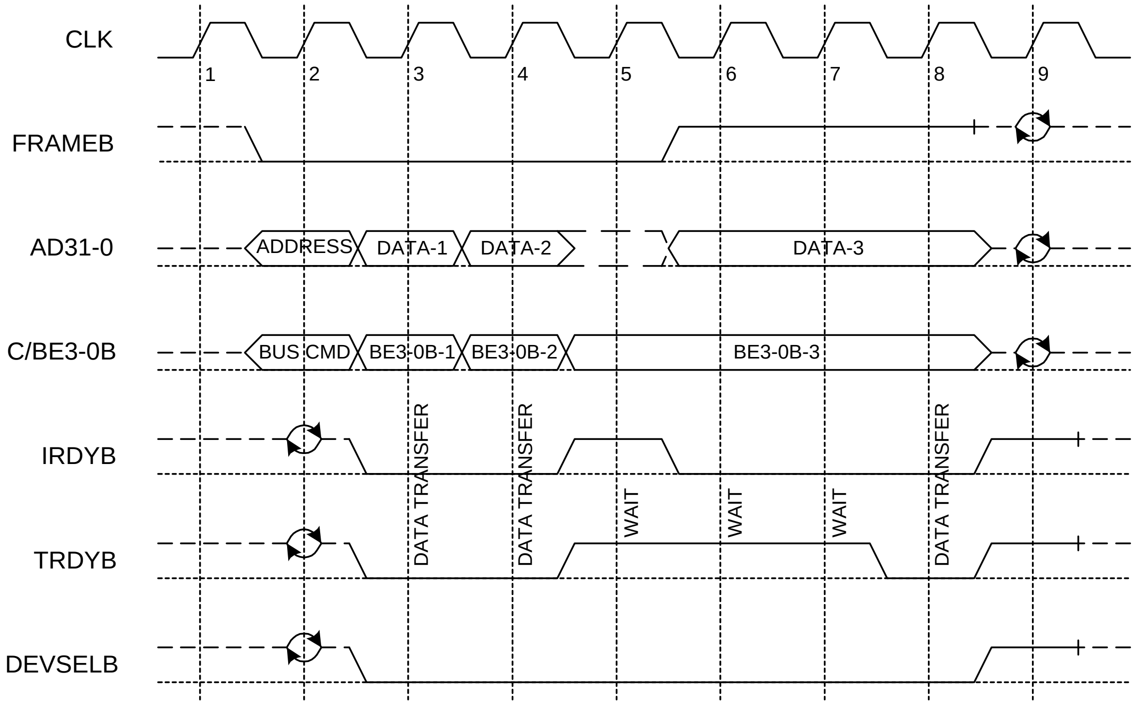


Figure 18. Memory Write below 4GB (32-bit address, 32-bit data; 32-bit slot)

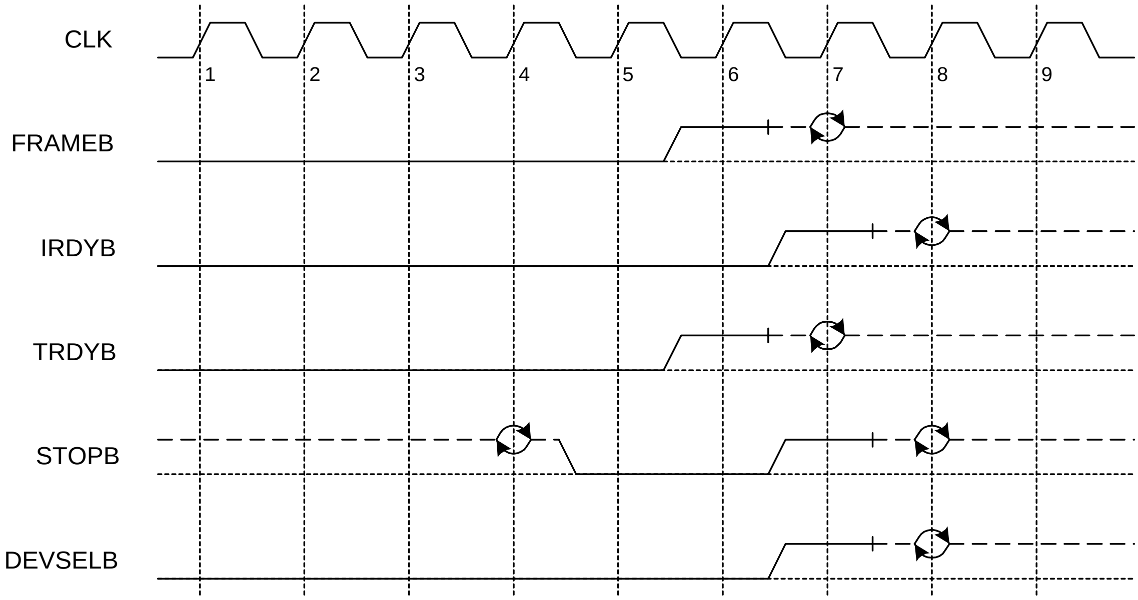


Figure 19. Target Initiated Termination - Disconnect

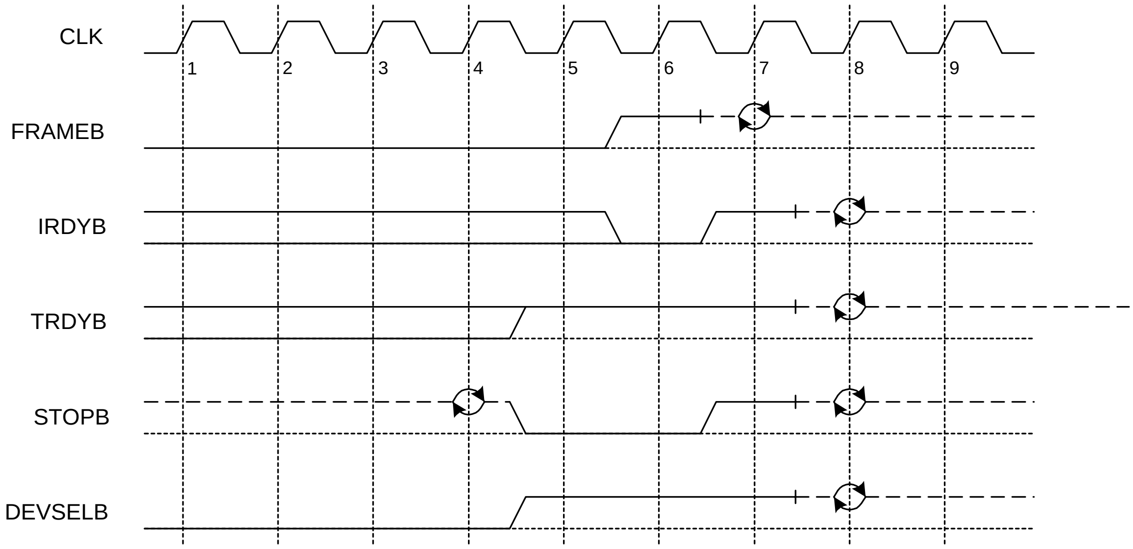


Figure 20. Target Initiated Termination - Abort

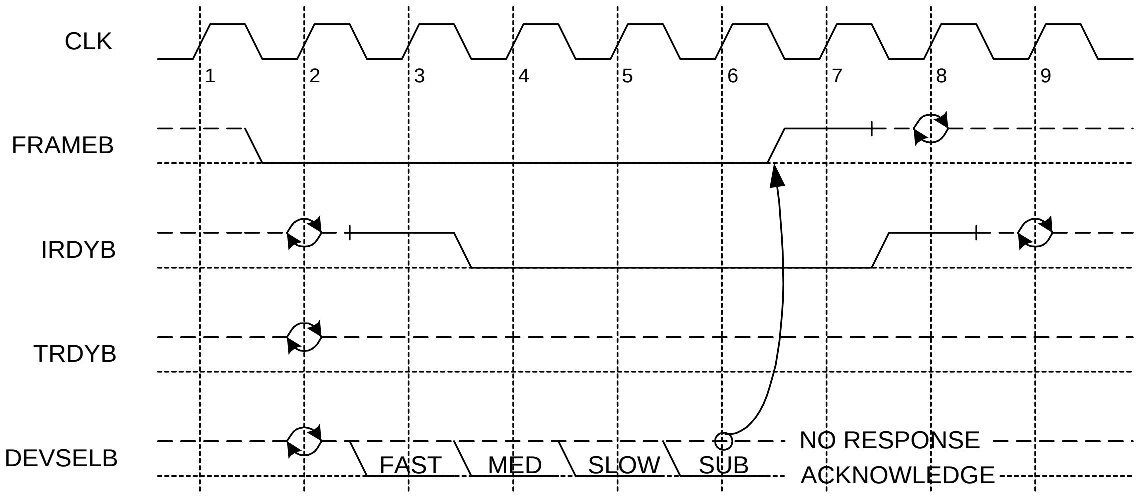


Figure 21. Master Initiated Termination - Abort

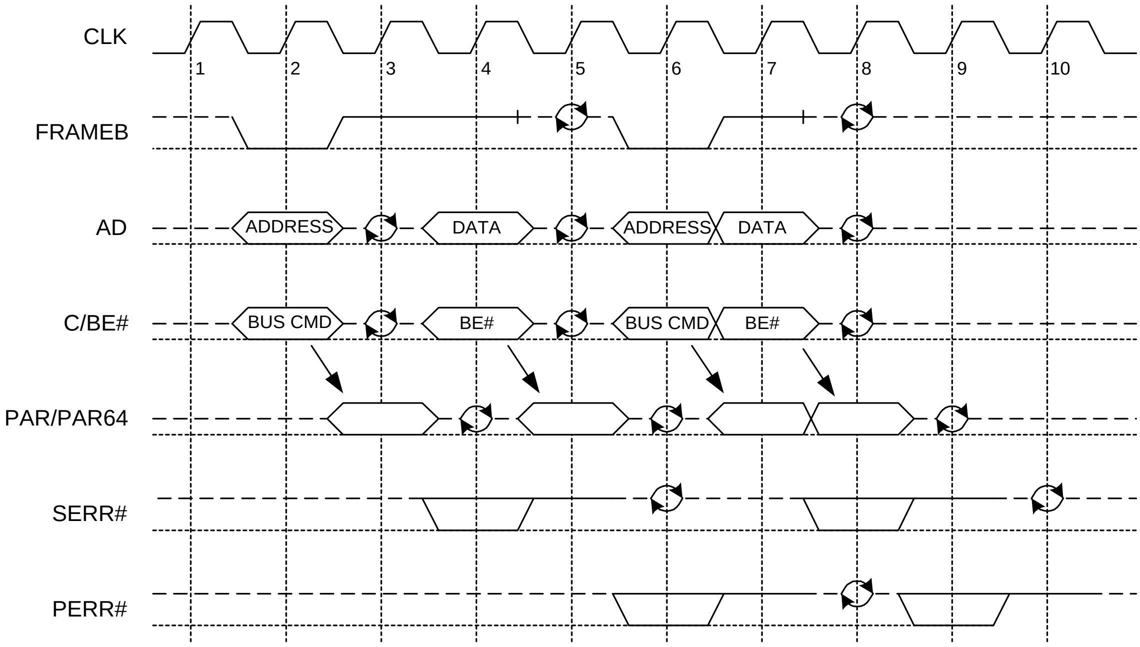


Figure 22. Parity Operation – One Example

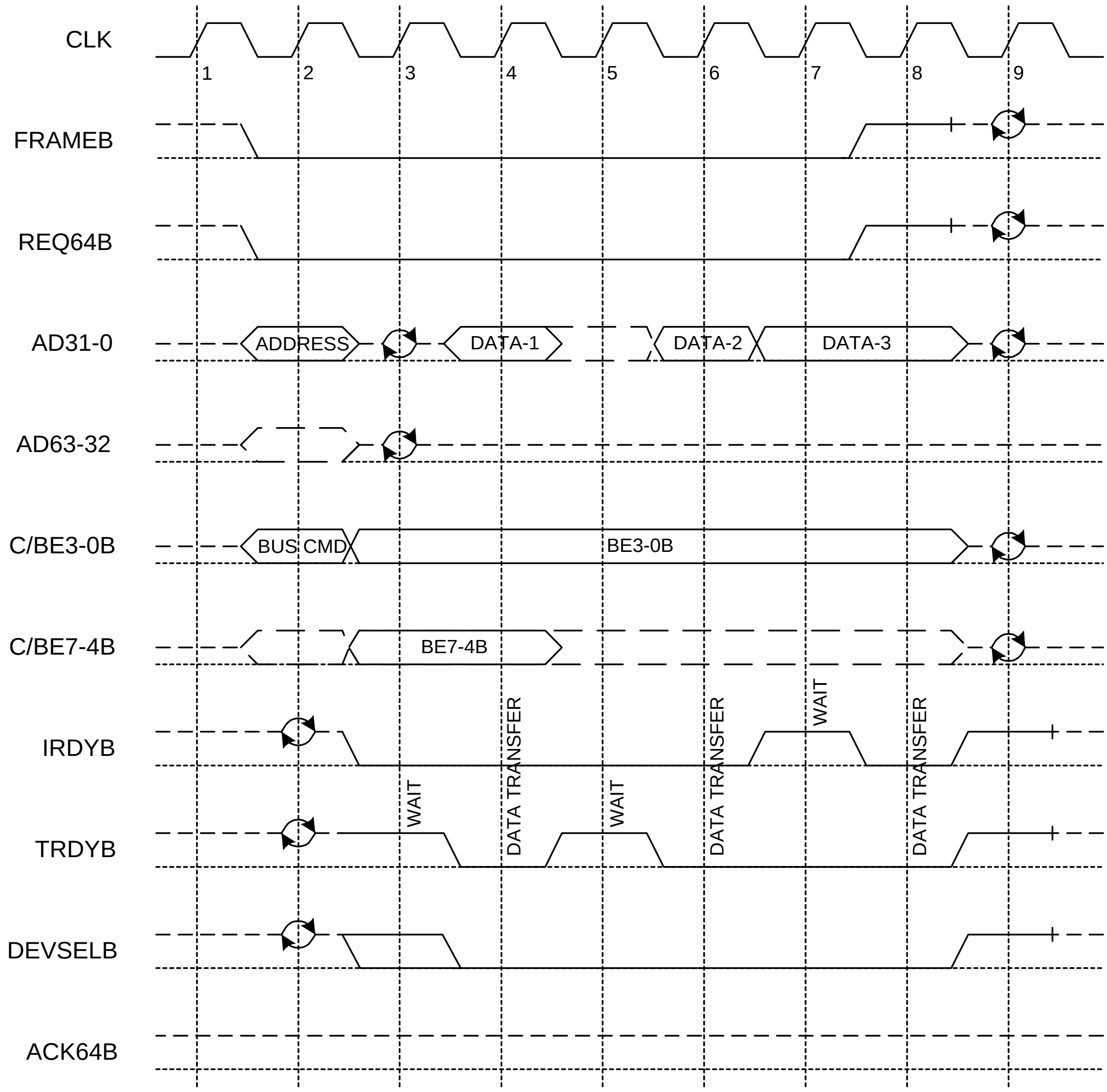


Figure 23. Memory Read Below 4GB (32-bit address, 32-bit data transfer granted; 64-bit slot)

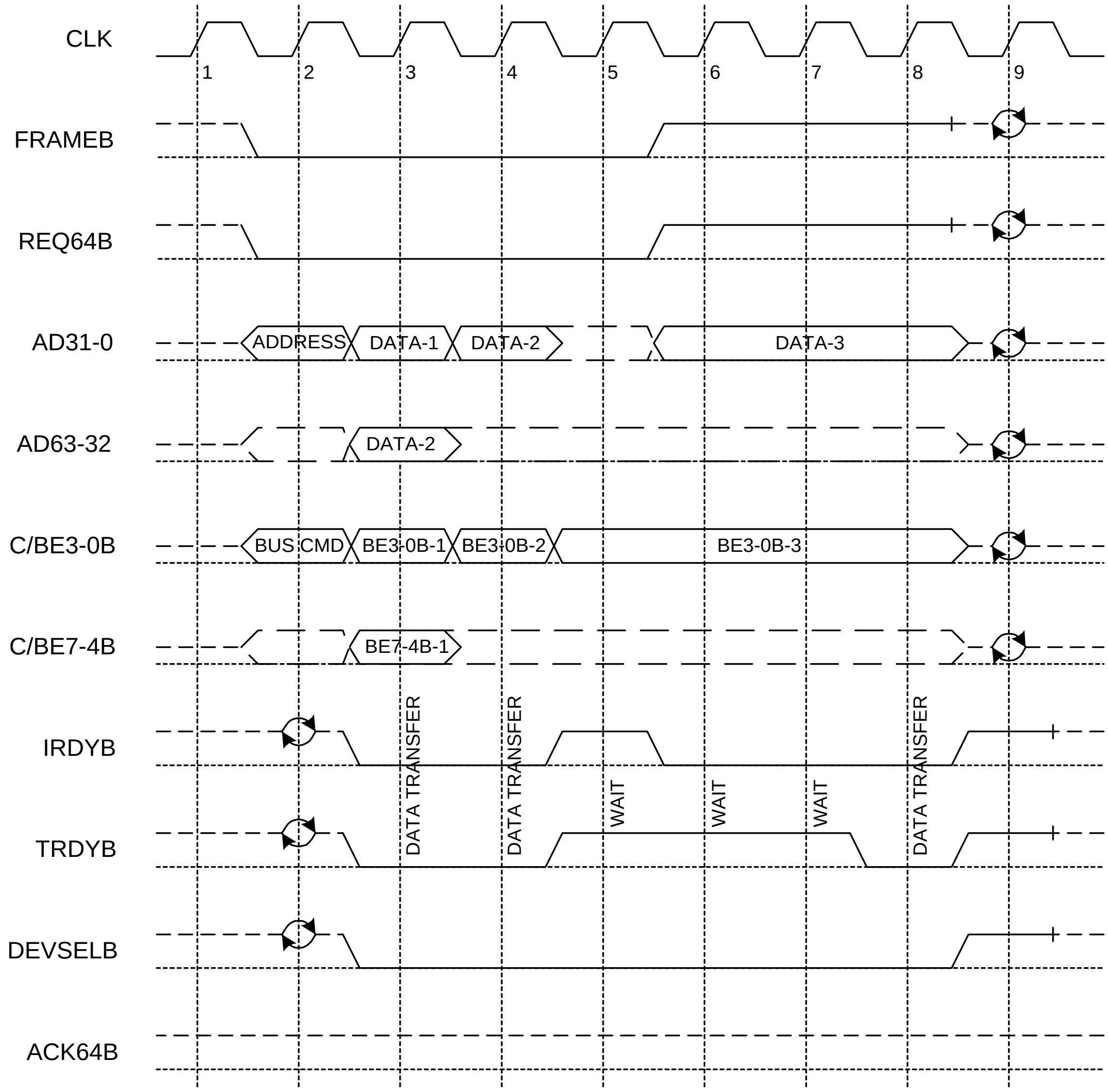


Figure 24. Memory Write below 4GB (32-bit address, 32-bit data transfer granted; 64-bit slot)

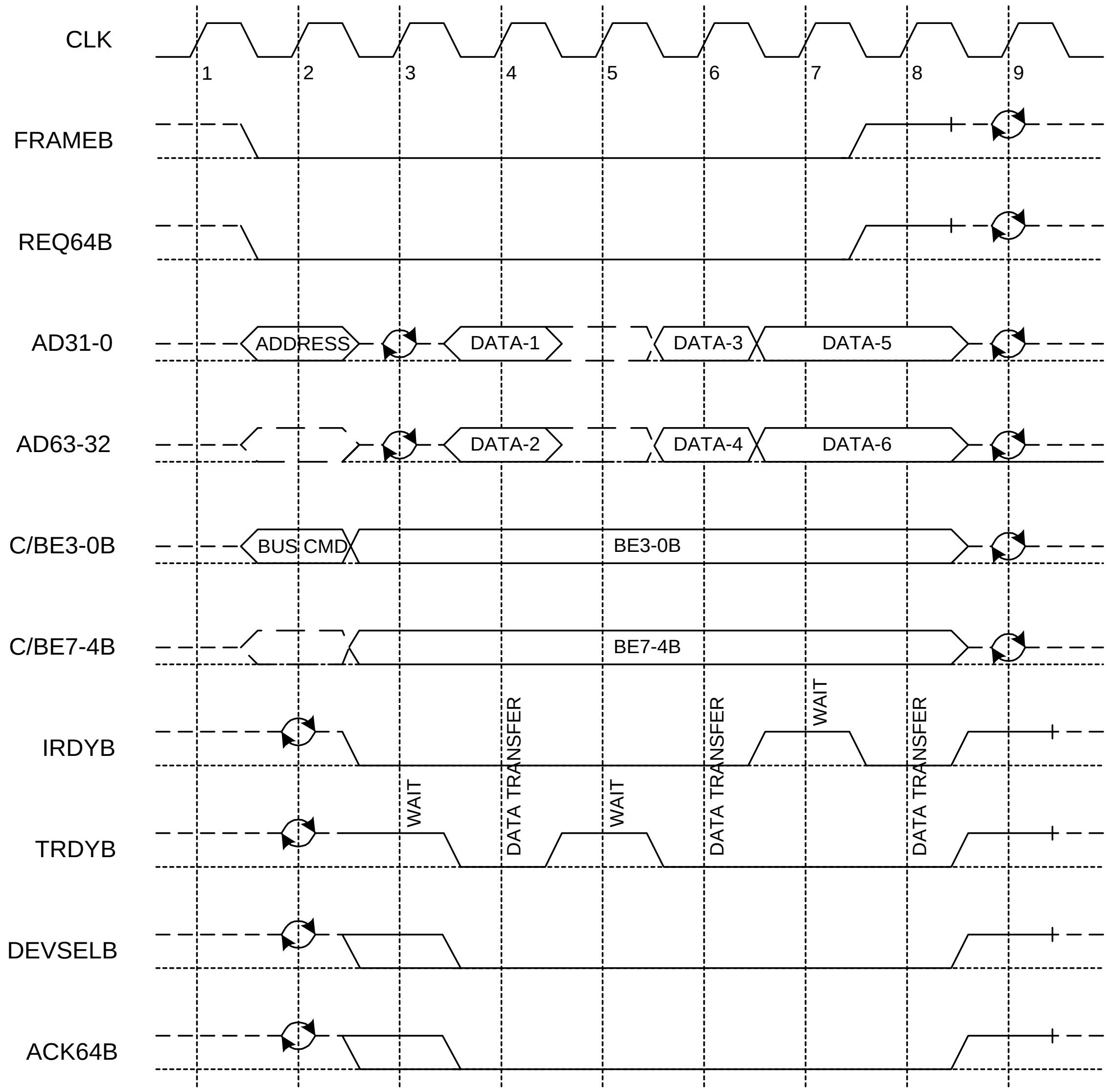


Figure 25. Memory Read below 4GB (32-bit address, 64-bit data transfer granted; 64-bit slot)

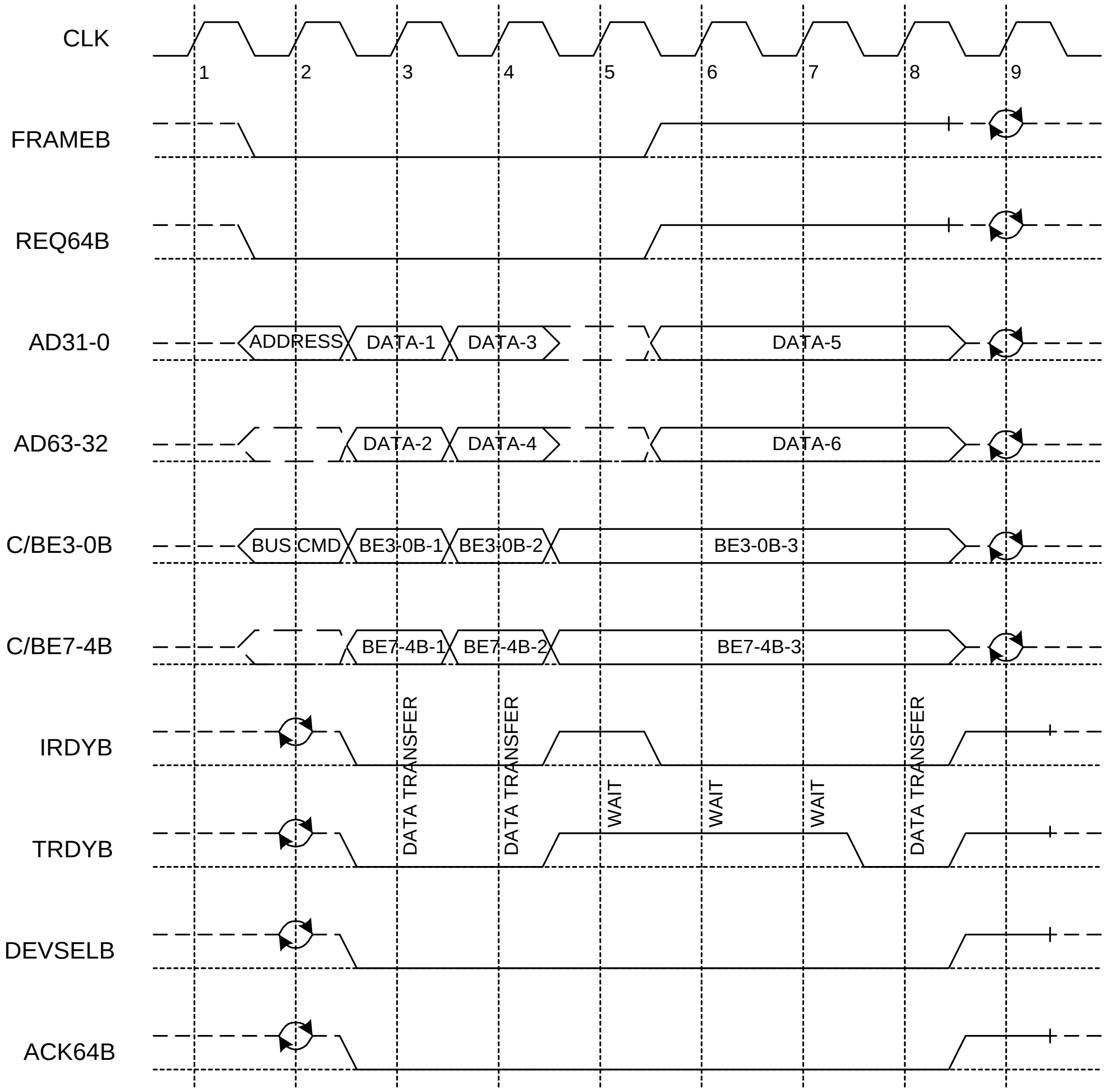


Figure 26. Memory Write below 4GB (32-bit address, 64-bit data transfer granted; 64-bit slot)

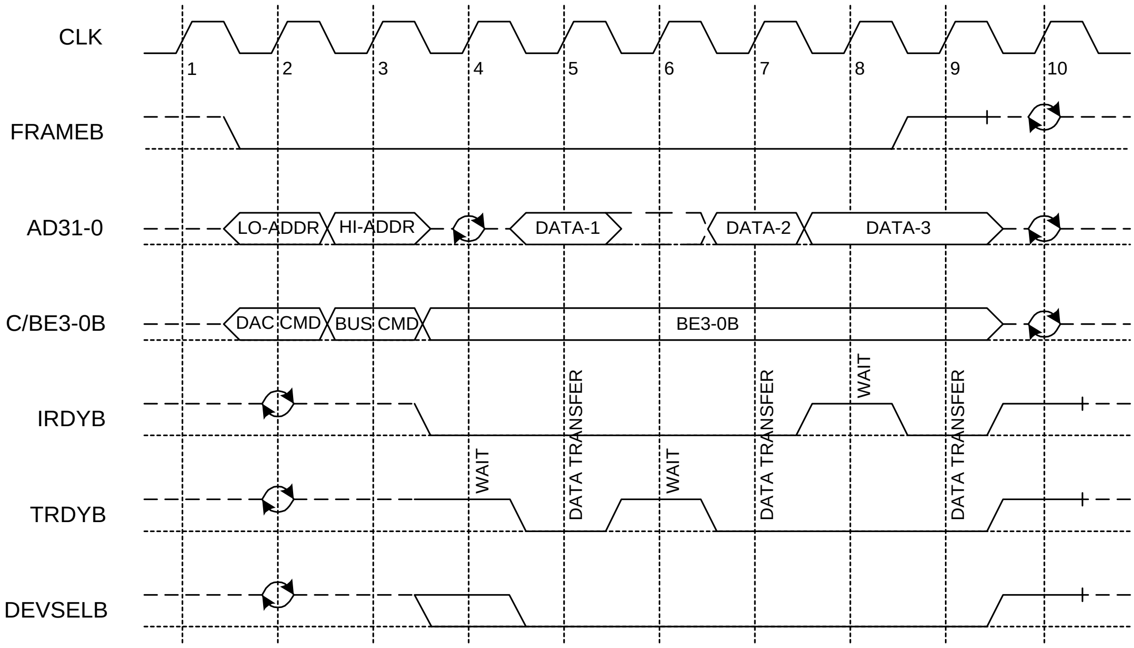


Figure 27. Memory Read above 4GB (DAC, 64-bit address, 32-bit data; 32-bit slot)

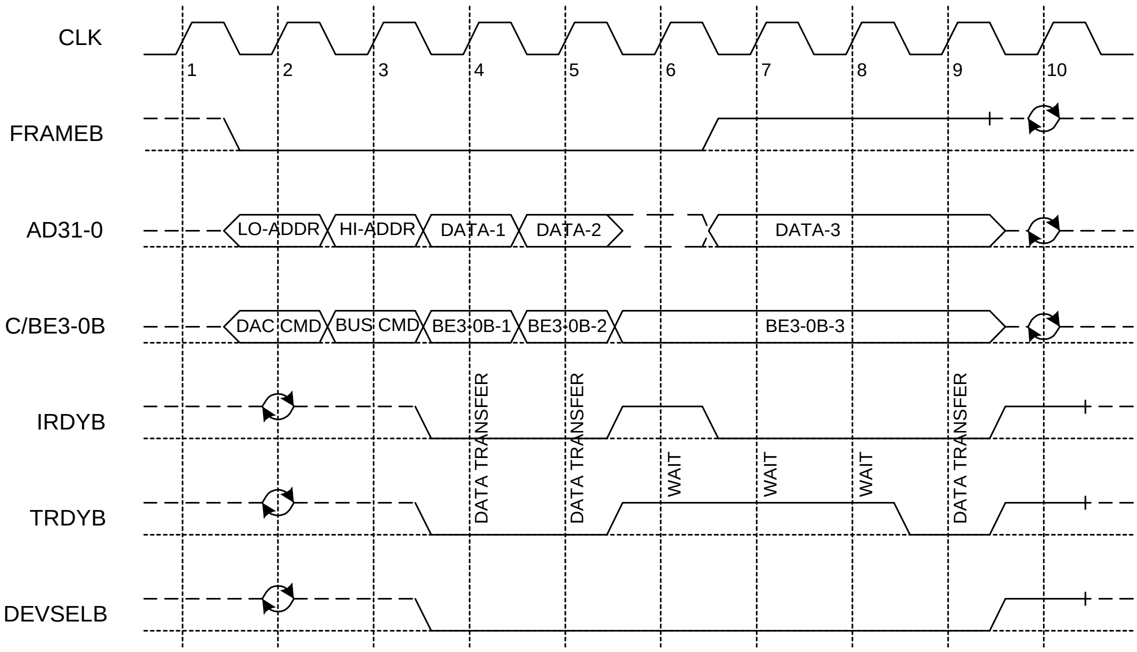


Figure 28. Memory Write above 4GB (DAC, 64-bit address, 32-bit data; 32-bit slot)

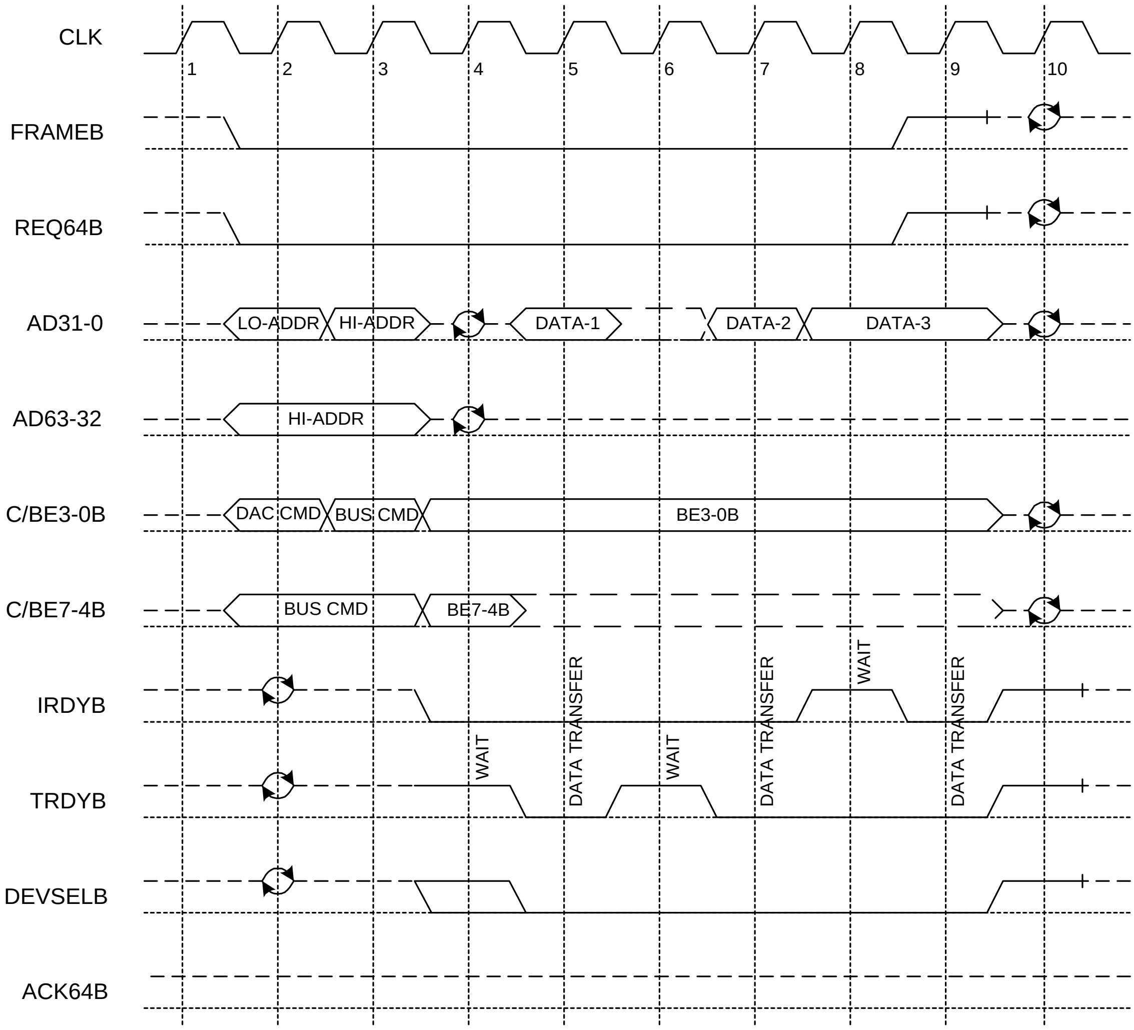


Figure 29. Memory Read above 4GB (DAC, 64-bit address, 32-bit data transfer granted; 64-bit slot)

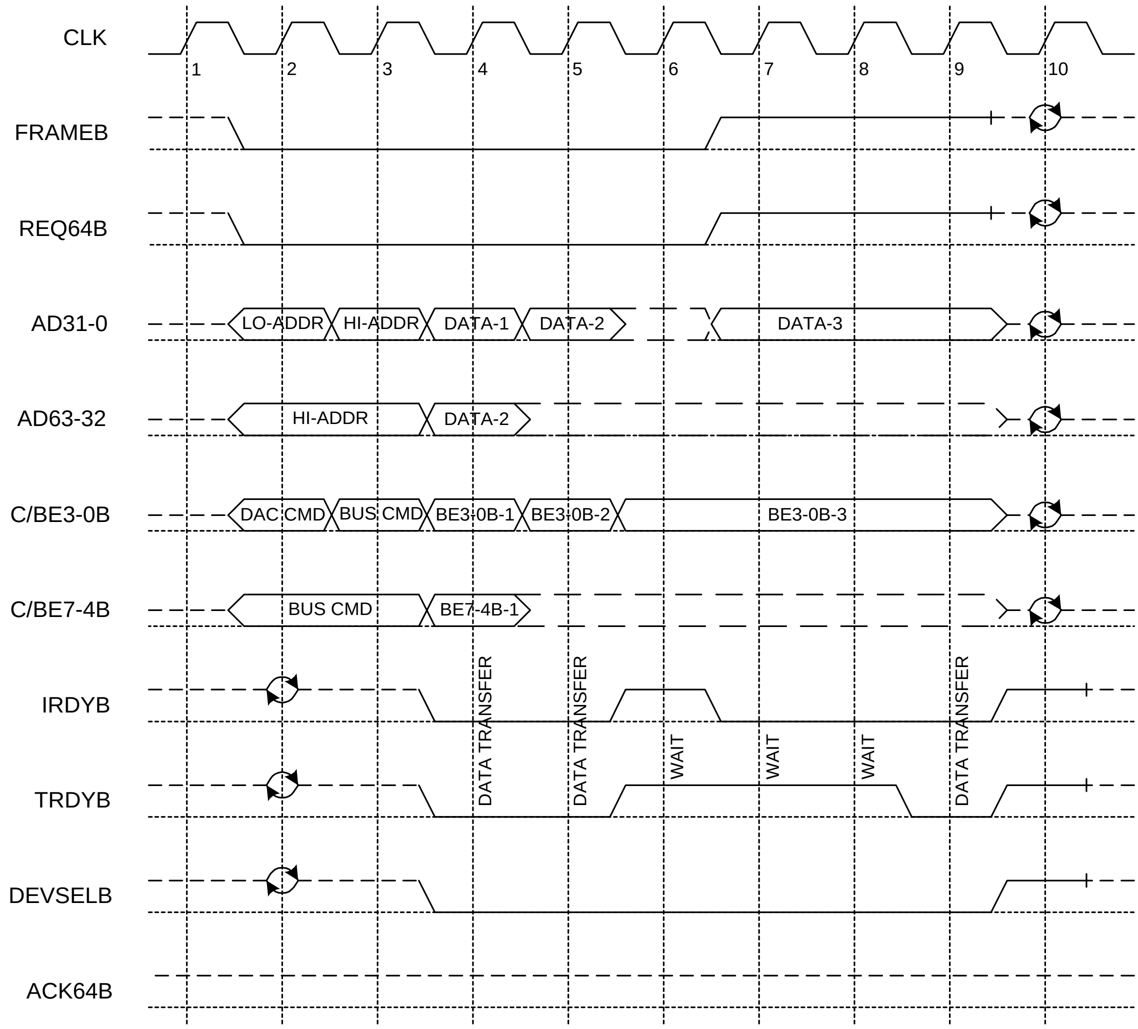


Figure 30. Memory Write above 4GB (DAC, 64-bit address, 32-bit data transfer granted; 64-bit slot)

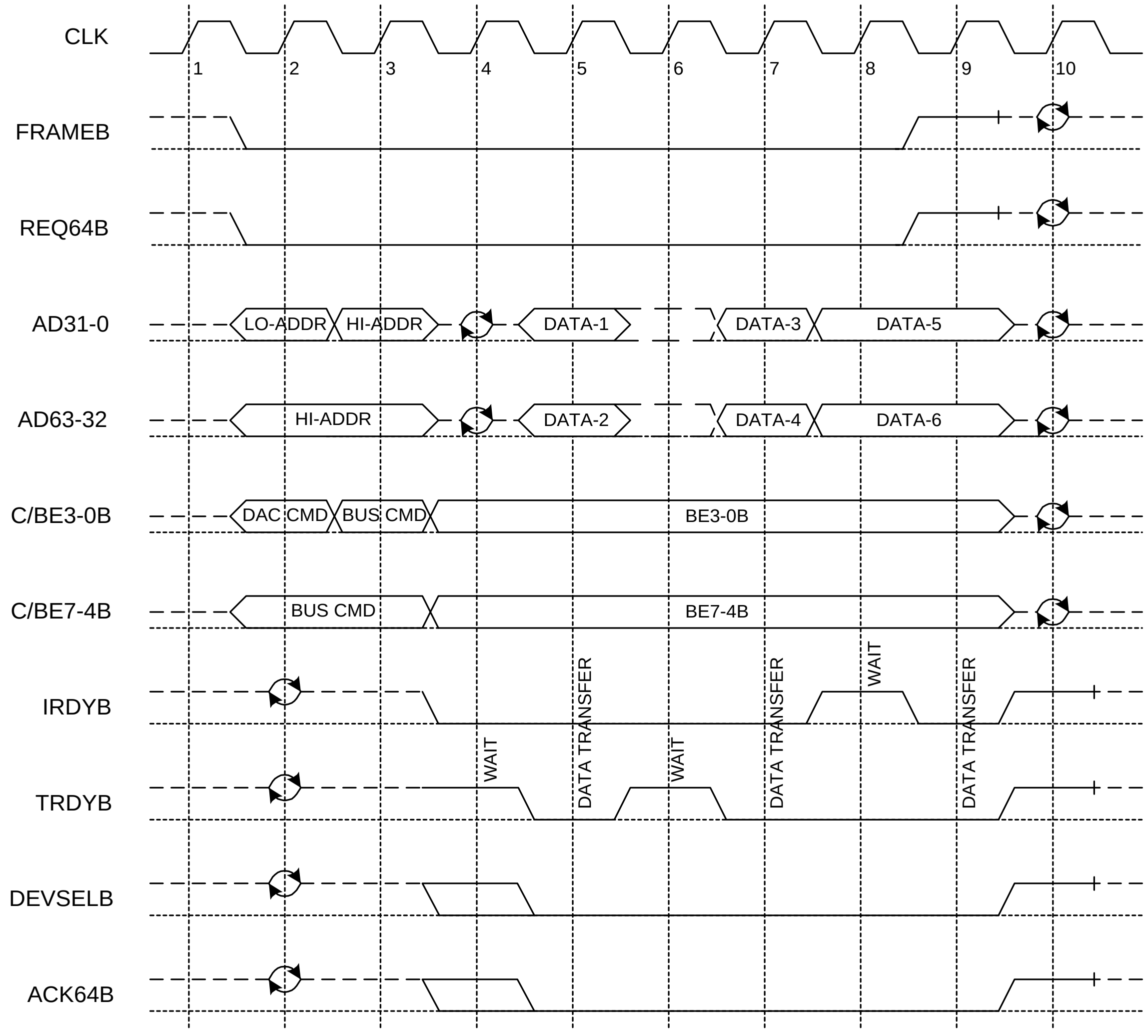


Figure 31. Memory Read above 4GB (DAC, 64-bit address, 64-bit data transfer granted; 64-bit slot)

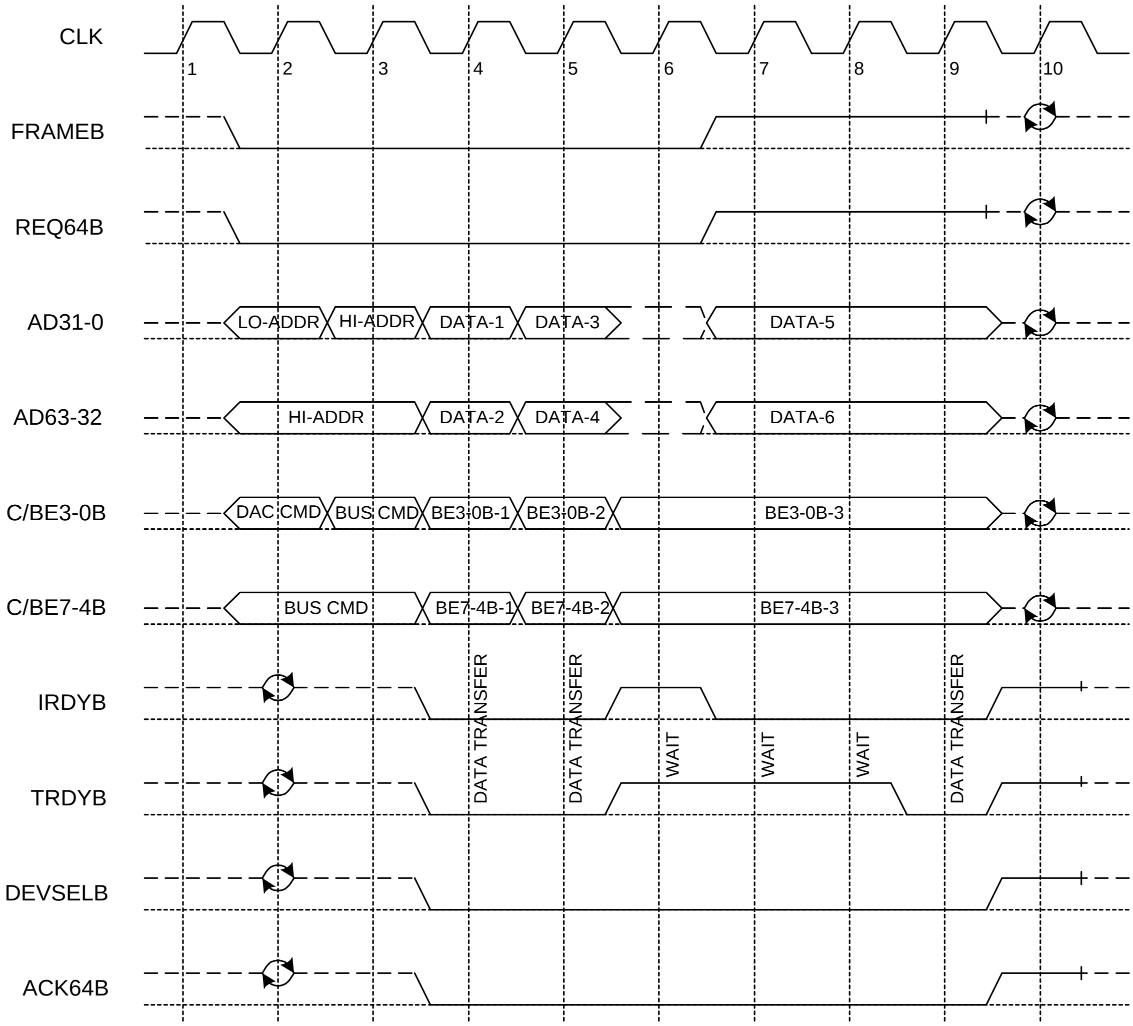
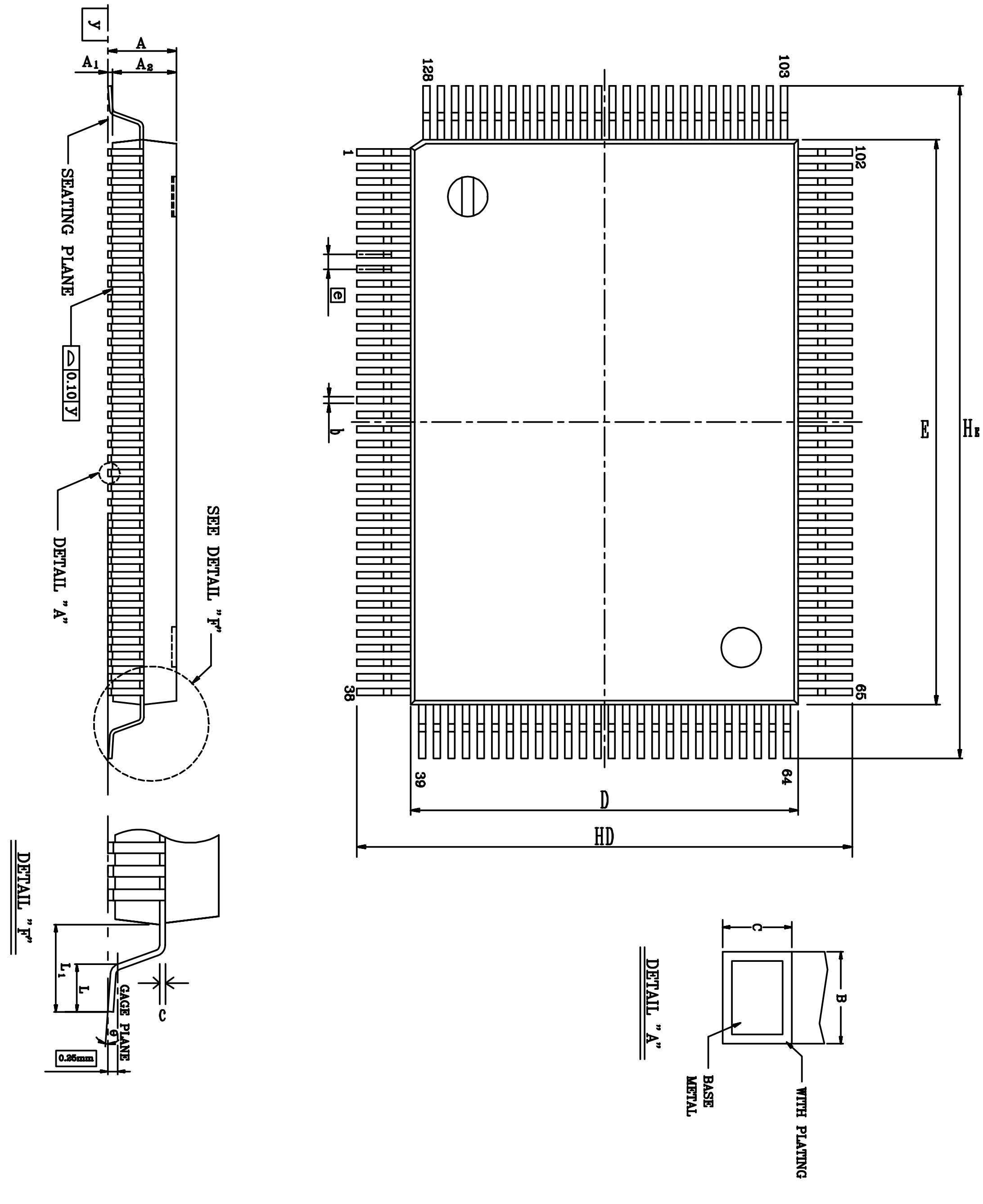


Figure 32. Memory Write above 4GB (DAC, 64-bit address, 64-bit data transfer granted; 64-bit slot)

8. Mechanical Dimensions

8.1. 128-Pin QFP Mechanical Dimensions



See the Mechanical Dimensions notes on the next page.

8.2. Notes for 128-Pin QFP Dimensions

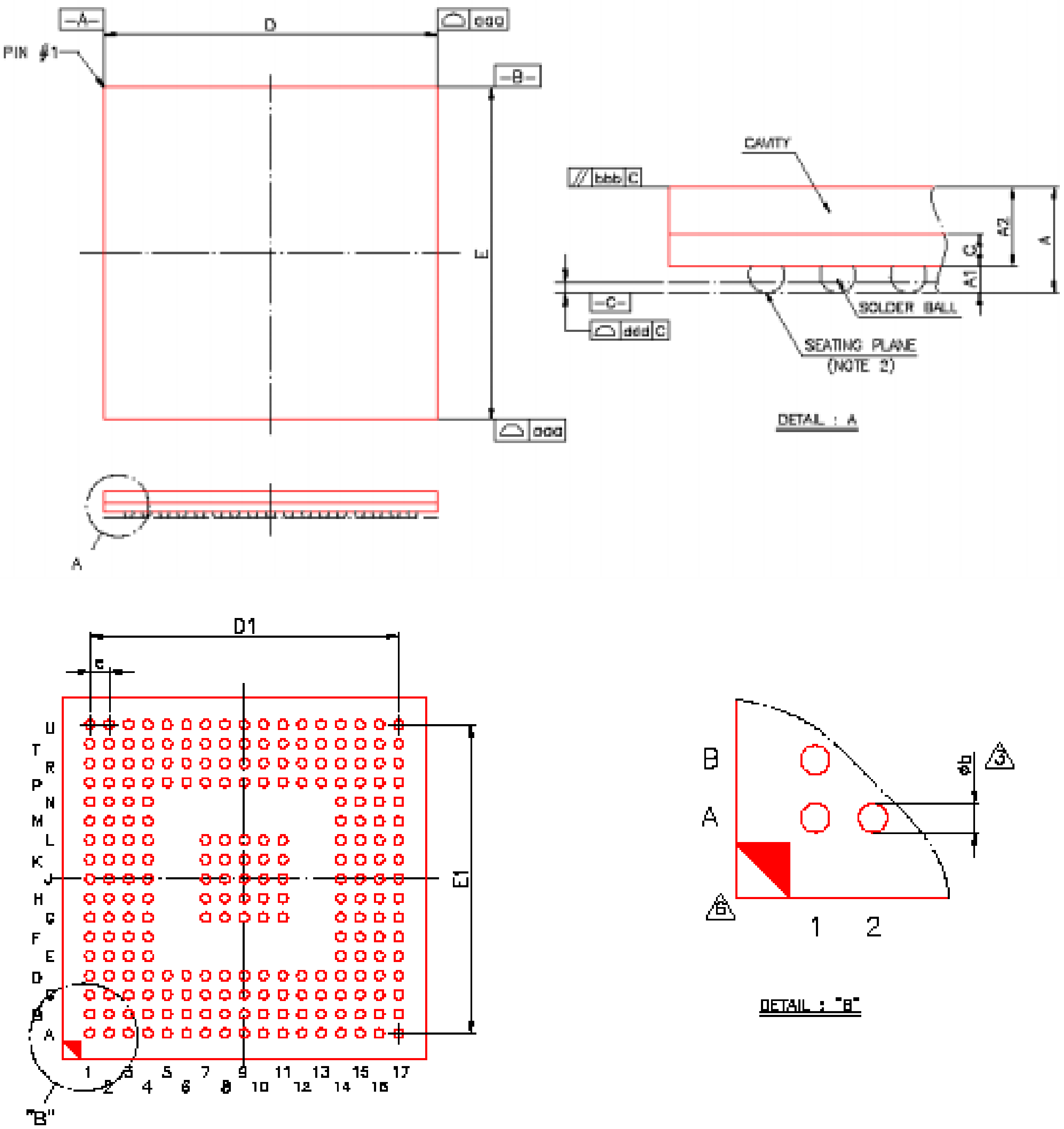
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Typical	Max	Min	Typical	Max
A	-	-	0.134	-	-	3.40
A1	0.004	0.010	0.036	0.10	**0.25**	0.91
A2	0.102	0.112	0.122	2.60	**2.85**	3.10
c	0.002	0.006	0.010	0.05	**0.15**	0.25
D	0.541	0.551	0.561	13.75	**14.00**	14.25
E	0.778	0.787	0.797	19.75	**20.00**	20.25
e	0.010	0.020	0.030	0.25	**0.5**	0.75
HD	0.665	0.677	0.689	16.90	**17.20**	17.50
HE	0.902	0.913	0.925	22.90	**23.20**	23.50
L	0.027	0.035	0.043	0.68	**0.88**	1.08
L1	0.053	0.063	0.073	1.35	**1.60**	1.85
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar rotrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. Should be based on final visual inspection.

TITLE: -CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	
		VERSION	
		PAGE	
CHECK		DWG NO.	Q128 - 1
		DATE	
REALTEK SEMICONDUCTOR CO., LTD			

8.3. 233-PIN TFBGA Mechanical Dimensions



See the Mechanical Dimensions notes on the next page.

8.4. Notes for 233-Pin TFBGA Dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.30	---	---	0.051
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.84	0.89	0.94	0.033	0.035	0.037
c	0.32	0.36	0.40	0.013	0.014	0.016
D	14.90	15.00	15.10	0.587	0.591	0.594
E	14.90	15.00	15.10	0.587	0.591	0.594
D1	---	12.80	---	---	0.504	---
E1	---	12.80	---	---	0.504	---
e	---	0.80	---	---	0.031	---
b	0.35	0.40	0.45	0.014	0.016	0.018
aaa	0.10			0.004		
bbb	0.10			0.004		
ddd	0.12			0.005		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	17/17			17/17		

NOTE :

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
5. REFERANCE DOCUMENT : JEDEC MO-205
6. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

9. Ordering Information

Table 20. Ordering Information

Part number	Package	Status
RTL8169S-32	128-pin QFP	
RTL8169S-64	233-pin TFBGA	

Realtek Semiconductor Corp.
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1F, No. 2, Industry East Road IX, Science-based
Industrial Park, Hsinchu, 300, Taiwan, R.O.C.
Tel: 886-3-5780211 Fax: 886-3-5776047
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